FPGA Implementation of Canonical Signed Digit Algorithm Based Floating Point Multiplication

A Project report submitted in partial fulfillment of the Requirements for the award of the degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ANIL NEERUKONDA INSTITUTE OF TECHNOLOGY AND SCIENCES (AUTONOMOUS)

(*Permanently Affiliated to AU, Approved by AICTE and Accredited by NBA & NAAC with 'A' Grade*)

Sangivalasa, Bheemili mandal, Visakhapatnam dist. (A.P)

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PRAGNANAM BRAHMA

ANITS

CERTIFICATE

This is to certify that the project report entitled **"FPGA Implementation of Canonical SignedDigit Algorithm Based Floating Point Multiplication"** submitted by **I.Hemanth (318126512139),Ch.Sravani(318126512129),G.BharatChandra(318126512125),P.Yashwanth (318126512167)** in partial fulfillment of the requirements for the award of the degree of **Bachelor of Technology** in **Electronics & Communication Engineering** of Andhra University, Visakhapatnam is a record of bonafide work carried out under my guidance and supervision.

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ABSTRACT

In today’s generation the requirement of very high-speed operations in processors is increased.To speed up the process of computation, arithmetic operations such as addition ,subtraction and multiplication are used in various digital circuits. Floating point multiplication is a criticaloperation in high power computing applications such as image processing, digital signal processing.

The main multiplier characteristics are good accuracy, increase in speed, reduction in area and less power consumption. As speed is always a constraint in the multiplication operation, increase in speed can be achieved by reducing the number of stages in the calculation process. Since the multiplier requires the longest delay among the basic operational blocks in digital system, the critical path is determined more by the multiplier. Furthermore, multiplier consumes much area and dissipates more power. Hence designing multipliers which offer either of the following design targets – high speed, lower power consumption, less area or evena combination of them is our prime concern.

The main aim of the project is to achieve the above design targets of a floating point multiplierusing Canonical Signed Digit (CSD) algorithm.

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LIST OF ABBREVATIONS

DSP	Digital Signal Processing
FPM	Floating Point Multiplication
CSD	Canonical Signed Digit
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
LSB	Least Significant Bit
IEEE	Institute of Electrical and Electronics Engineers
RCA	Ripple Carry Adder
CLA	Carry Look -Ahead Adder
CSA	Carry Save Adder
CA	Carry-Select Adder
SPST	Spurious Power Suppression Technique
UT	Urdhva Triyakbhyam
DDR	Double Data Rate
LUT	Look Up Tables
PLL	Phase-Locked Loop
HR	High Range
ODT	On-Die Terminations
PHY	Physical Layer
MiB	mebibyte
RTL	Register Transfer Level
EDA	Electronic Design Automation

CHAPTER1

INTRODUCTION

The multiplication operation is one of the important operations in digital signal processing (DSP) used in applications such as the Discrete Fourier Transform, Fast Fourier Transform, convolution or digital filters. Thus, there has been a continuous research for refining predefined multipliers and developing new approaches for efficient multiplier architecture. There are many existing multiplier architectures such as Shift and Add multiplier, Booth multiplier, Wallace tree multiplier, Array multiplier etc. Shift and Add multiplier is the simplest among all however, large number of gates are required making time inefficient architecture. High performance multipliers are preferred with regular structures or reduced number of partial products. The array multiplier and Wallace tree multiplier are based on the arrangement of adders aiming reduction in overall critical path of the multiplication operation.

Many significant amounts of work have been published using the concept of Vedic mathematics, obtaining efficient multiplier, divider, squaring and cube architectures. The efficiency of multiplier is based on factors: (i) larger operation is reduced to the smaller operation. (ii) the speed of addition operation in accumulation of partial products is increased using carry select adders. The multiplier architecture is found to be efficient as compared to the state-of-art Vedic multipliers. The reduction in number of stages in a Vedic multiplication process leads to significant reduction in the propagation delay along with switching power consumption. The multiplication operation is based on Urdhva Tiryagbhyam algorithm of Vedic mathematics.

Generally, most of the multipliers consumes much area, consumes more power and work with less accuracy. hence designing multipliers which offer either of the following design targets-high speed, low power consumption, less area or even a combination of all these is of substantial research interest.

1.1 PROJECT OBJECTIVE

The main aim of the project is to simulate and implement FPM(Floating Point Multiplication) multiplication using CSD(Canonical Signed Digit)algorithm andcompare it with existing multipliers. Vivado design suite is used for simulation. Synthesis and implementation is done using basys 3 DDR board, which is ready to use digital circuit development platform based on the latest Artix -7 Field Programmable Gate Array (FPGA) from Xilinx. The performance is compared in terms ofpower, area and delay

1.2 PROJECT OUTLINE

This project report is presented over the 4 remaining chapters. Chapter 2presents Floating Point Multiplication and provides the fundamentals of various adders and multipliers. Chapter 3 explains about Canonical Signed Digit (CSD) algorithm.Chapter 4 describes simulation and synthesis tools necessary to simulate and synthesize the given hardware using Verilog Hardware Description Language. Chapter 5 presents the simulation results which are simulated using Vivado Design Suite simulator. Also the synthesis and implementation results are carried out using basys 3 DDR board, which is ready to use digital circuit development platform based on the latest Artix -7 Field Programmable Gate Array (FPGA) from Xilinx. Finally, the results of the project work and conclusions are drawn.

CHAPTER 2
FLOATING POINT MULTIPLICATION

2.1 NUMBER SYSTEM

The number system is a system generally used for representing or expressing numbers. It is a mathematical notation which can be a combination of numbers and alphabets. There are various kinds of number systems like binary, decimal, octal, hexadecimal based on the base. The base is also called as “radix”.

2.1.1FIXED POINT

The term 'fixed point' refers to the corresponding manner in which the numbersare represented. A fixed point decimal number system has a limited number of digits anda decimal point in a fixed location.

To define a fixed-point type conceptually, all we need are two criterions:width of the number and binary point position within the number

We will use the notation fixed <w, b> where w stands for the number of bits used as a whole (the Width of a number), and b stands for the position of binary point counting from the Least Significant Bit(LSB) (counting from 0).

For example, fixed<8,3> denotes an 8-bit fixed point number, of which 3 right most bits are fractional. Therefore, the bit pattern:

represents a real number:

00010.110

= 1 * 2^1 + 1 * 2^-1 + 1 * 2^-2

= 2 + 0.5 + 0.25= 2.75

Fixed point numbers are indeed an in depth relative to integer representation. The two only differs within the position of binary point. In fact, you would possibly even considerinteger representation as a "special case" of fixed-point numbers, where the binary pointis at position 0. All the arithmetic operations a computer can operate integer can thereforebe applied to fixed point number also. The disadvantage of number, is than in fact the loss of range and precision. For example, in a fixed representation, our fractional part is only precise to a quantum of 0.5. We cannot represent number like 0.75. We can represent 0.75 with fixed, but then we lose range on the integer part.

2.1.2 FLOATING POINT

The floating point is the arithmetic using the representation of real numbers as an approximation in supporting trade-off between range and precision. For this reason,floating-point computation is usually found in systems which include very small and really large real numbers, which require fast processing times.

In computers the real numbers are represented in floating point (FP) format. Usually this suggests that the amount is split into exponent and fraction, which is additionally referred to as significand or mantissa. A scientific notation with a symbol , exponent, mantissa called floating point representation is employed for the important numbers. Its format is Real number→mantissa×base^exponent

Where significand is an integer, base is an integer greater than or adequate to two, and exponent is additionally an integer. For example:

1.2345 = 12345 x 10^-4

2.1.3 SINGLE PRECISION FLOATING POINT MULTIPLICATION

Most modern computers use Institute of Electrical and Electronics Engineers (IEEE) 754 standard for representation of floating-point numbers. One of the most commonly used formats is the binary32 format of IEEE 754:

Sign bit-1 bit Exponent-8 bits

Significand/mantissa-23 bits

Note that exponent is encoded using an offset-binary representation, which suggests it is often off by 127. So, if usually 10000000 in binary would be 128 in decimal, in single- precision the worth of exponent is:

exponent=128−offset=128−127=1

2.1.4 FLOATING POINT MULTIPLICATION

From the literature, it is observed that various multipliers such as Array multiplier, Vedic multiplier and Radix based multipliers are involved in multiplication.

In general, Floating Point Multiplication (FPM) of two numbers involves four steps:

• Non-signed multiplication of mantissas

• Normalization of the result

• Addition of the exponents, taking into account the bias.

• Calculation of the sign.

Let us consider two numbers

a=6.96875

b=-0.3418

Normalized values and biased exponents:

a=6.96875=1.7421875×2^2 b=−0.3418=−1.3672×2^−2

The exponents:

Exponent a=2 Exponent b=−2

The numbers in IEEE754 *binary32*: a=01000000110111110000000000000000(binary32)

=10111110101011110000000001101001(binary32)

The mantissa could be rewritten as following totaling 24 bits per operand:

Mantissa a=1.101111100000000000000002Mantissa b=1.010111100000000011010012

Their multiplication totals in 48 bits:

Mantissa=1.00110000111000101011011011101110000000000000000002

Which has to be truncated to 24 bits:

mantissaa×b=1.001100001110001010110112=2.381918668746948242187510

The exponents 2 and -2 can easily be summed up so only last thing to do isto normalize fraction which means that the resulting number is:

a×b=−2.3819186687469482421875=−1.19095933437347412109375×21

Which could be written in IEEE 754 *binary32* format as:

a×b=01000000000110000111000101011011binary32

2.2 ADDERS

An adder is a digital circuit which performs addition of numbers. In many computers and other types of processors, adders are used in the ALU and also in other parts of the processors. Adders are used to calculate addresses, table indices and are also used to perform increment and decrement operations. The most common adders operate on binary numbers.

2.2.1 HALF ADDER(HA)

A combinational circuit that performs the addition of two single bits is called Half Adder. The half adder adds two binary digits *A* and *B*. It has two outputs, sum and carry.The carry signal represents an overflow into the next digit of a multi-digit addition. To design a simple half adder we use an XOR gate for sum and an AND gate for carry.

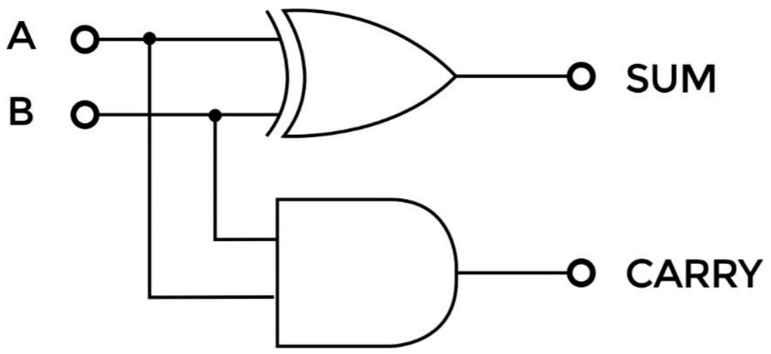


FIG 1 Half adder logic diagram.

Table 1 Half adder truth table

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

2.2.2 FULL ADDER(FA)

A combinational logic circuit that performs the addition of three single bits and produces two outputs is called Full Adder. A, B and Cin are the inputs. Sum and C-OUT are the outputs. In half adder we can add 2-bit binary numbers but we cannot add carry bit along with the two binary numbers. But in full adder we can carry in bit along with two binary numbers**.**

Table 2 Full adder truth table

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

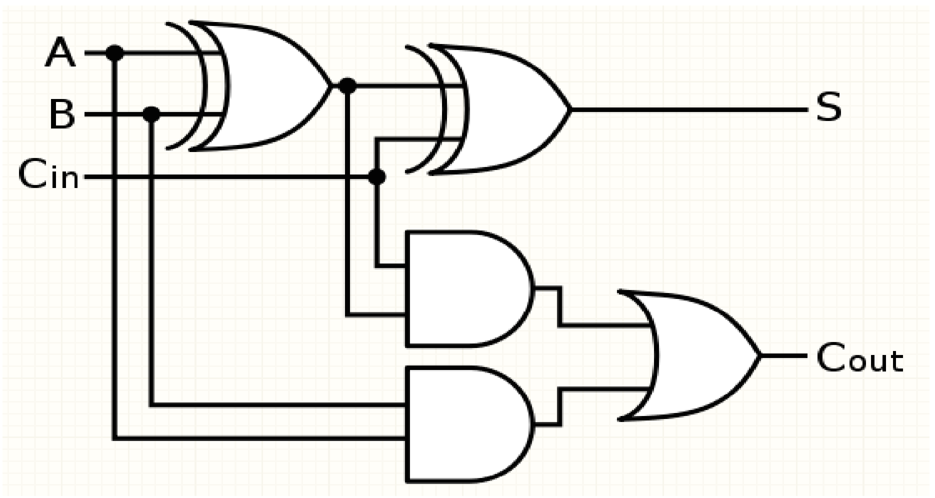


Fig 2 Full adder logic diagram

2.2.3 RIPPLE CARRY ADDER(RCA)

Ripple carry adder is a structure of multiple full adders is cascaded in a manner to gives the results of the addition of an n bit binary sequence and the carry will be generated at every full adder stage. These carry output at each full adder stage is forwarded to its next full adder and applied as a carry input to it. This process continues up to its last stage of adder circuit. So, each carry output bit is rippled to the next stage of a full adder and hence named as “RIPPLE CARRY ADDER”. The most important feature of it is to add the input bit sequences if the sequence is 4 bit or 5 bit or any.

There are various types in ripple-carry adders. They are:

- 4-bit ripple-carry adder
- 8-bit ripple-carry adder
- 16-bit ripple-carry adder

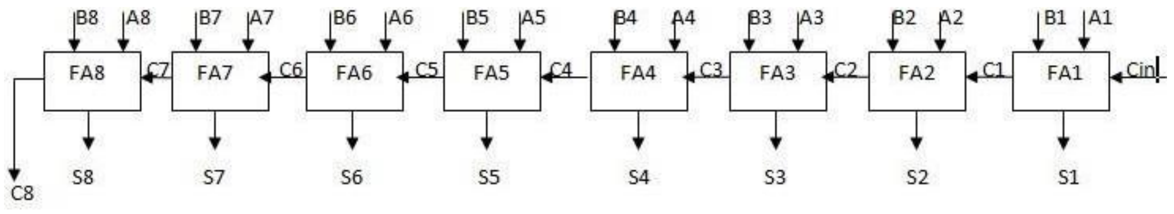
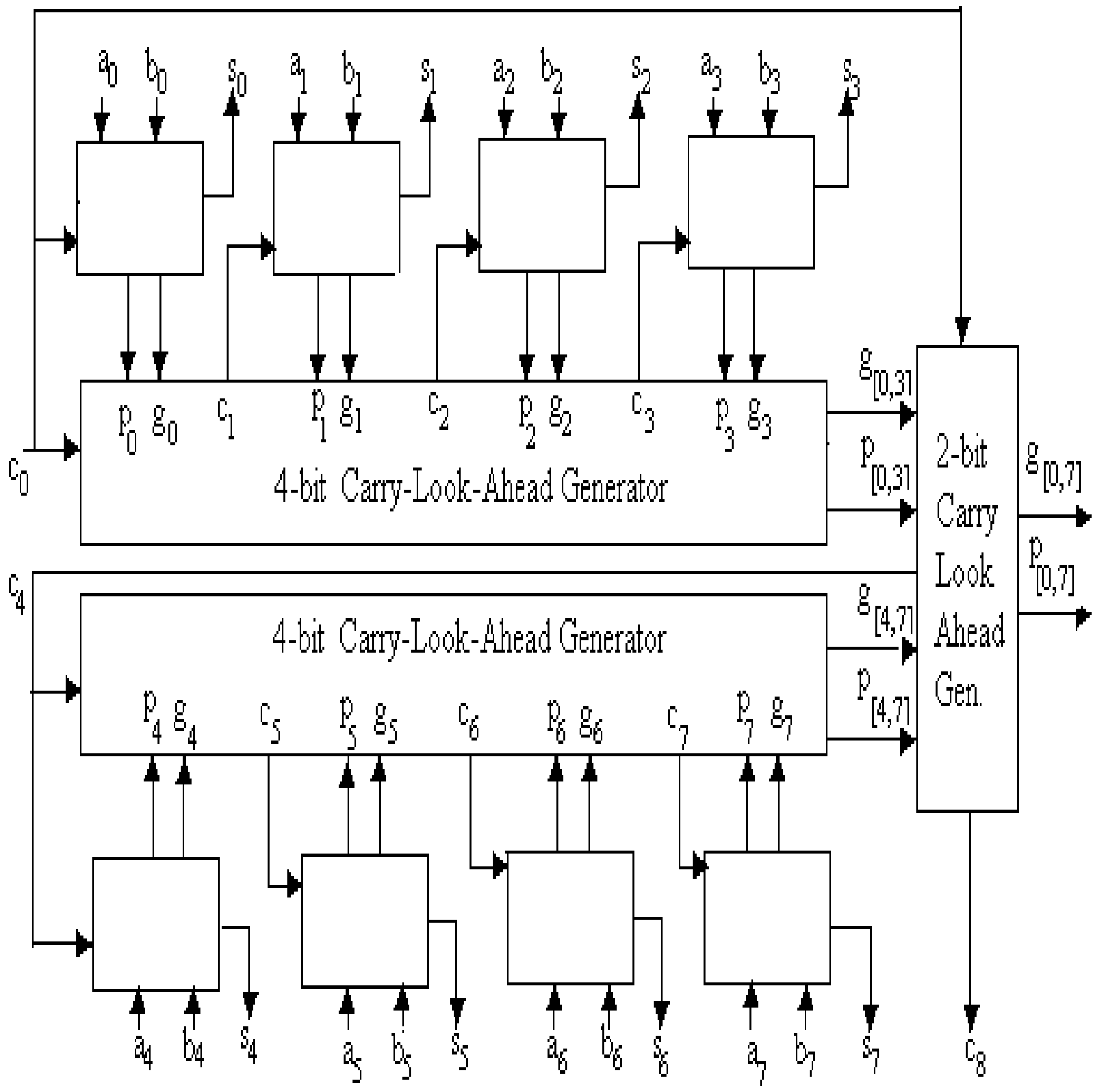


Fig 3 Ripple Carry adder logic diagram

2.2.4 CARRY LOOK AHEAD ADDER(CLA)

In ripple carry adders, for each adder block, the two bits that are to be added are available instantly. However, each adder block waits for the carry to arrive from its previous block.So, it is not possible to generate the sum and carry of any block until the input carry is known. The block waits for the block to produce its carry. So, there will be a considerable time delay which is carry propagation delay.

A carry look-ahead adder reduces the propagation delay by introducing more complex hardware. In this design, the ripple carry design is suitably transformed such that the carry logic over fixed groups of bits of the adder is reduced to two-level logic.



a_0 b_0 s_0 a_1 b_1 s_1 a_2 b_2 s_2 a_3 b_3 s_3
p_0 g_0 c_1 p_1 g_1 c_2 p_2 g_2 c_3 p_3 g_3
c_0
4-bit Carry-Look-Ahead Generator
$g_{[0,3]}$
$p_{[0,3]}$
2-bit Carry Look Ahead Gen.
$g_{[0,7]}$
$p_{[0,7]}$
c_4
4-bit Carry-Look-Ahead Generator
$g_{[4,7]}$
$p_{[4,7]}$
p_4 g_4 c_5 p_5 g_5 c_6 p_6 g_6 c_7 p_7 g_7
a_4 b_4 s_4 a_5 b_5 s_5 a_6 b_6 s_6 a_7 b_7 s_7 c_8

Fig 4 Carry look ahead adder

2.2.5 CARRY SAVE ADDER(CSA)

A carry save adder is a type of digital adder used in computer microarchitecture to compute the sum of three or more n-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is asequence of partial sum bits and another which sequence of carry bits.

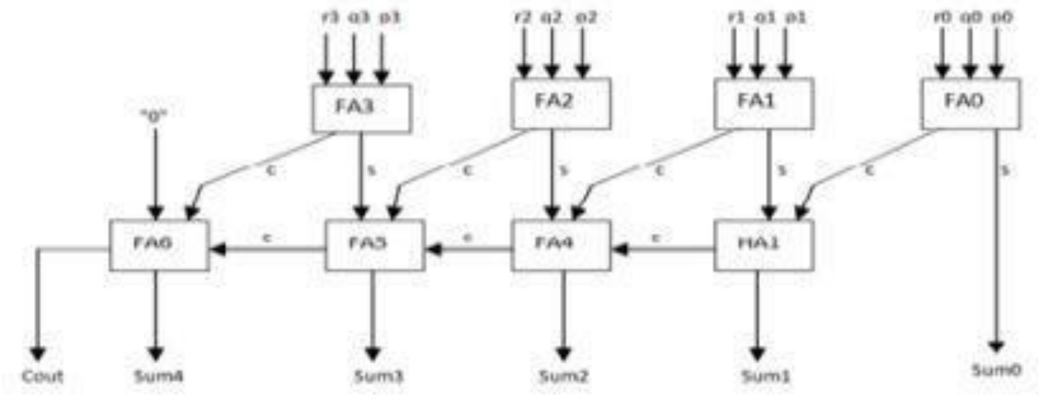


Fig 5 Carry save adder

2.2.6 CARRY- SELECT ADDER(CA)

In electronics, a carry-select adder is a particular way to implement an adder which is a logic element that computes the (n+1)-bit sum of two n-bit numbers.

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders), in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the tworesults are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer once the correct carry-in is known.

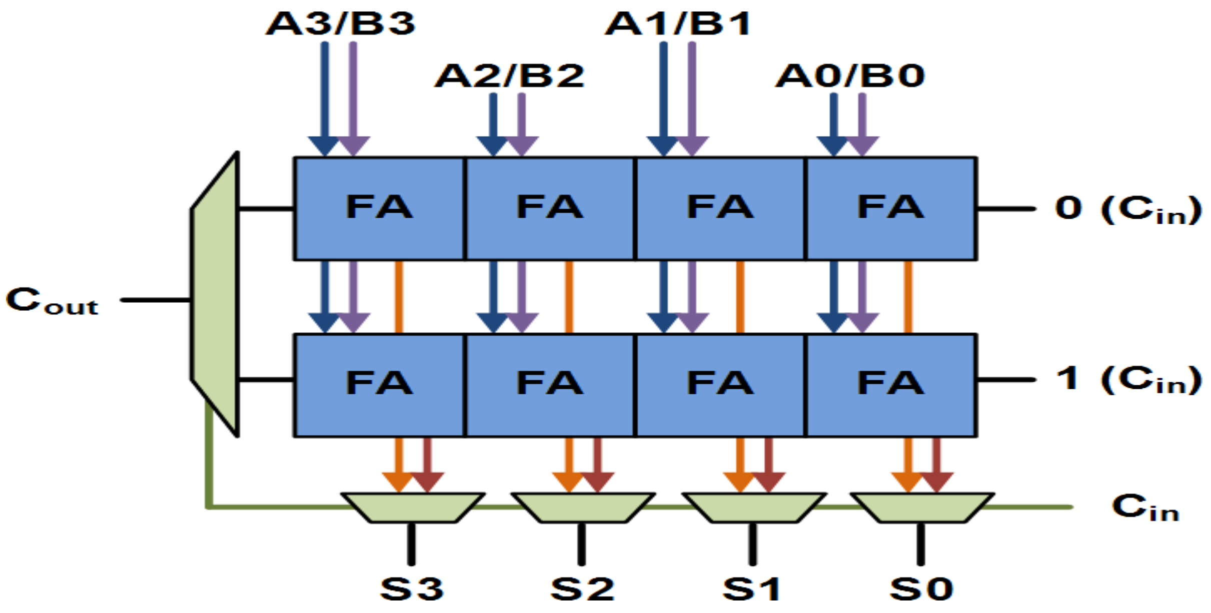


Fig 6 Carry select adder

Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

2.2.7 SUPERIOUS POWER SUPPRESSION TECHNIQUE ADDER(SPST)

Adder is a circuit that is combinational and calculates the sum of three(full adder) or two (half adder) inputs. Full adder can be cascaded to produce n-stages of adder. This cascaded adder structure is called as parallel adder. The sum and carry of any stage cannot be calculated until the input carry occurs, this leads to a delay in the additionprocess. In order to overcome the delay, carry look ahead adder is proposed which is said to be a fast adder. To improve the speed of carry, look ahead adder, Spurious Power Suppression Technique (SPST) is used.

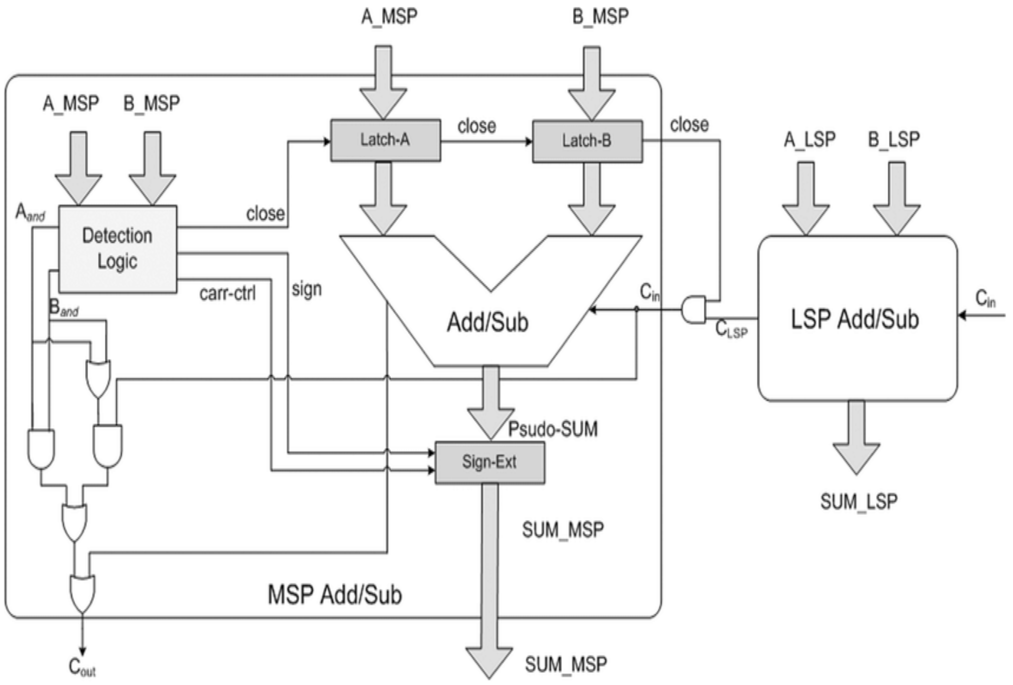


Fig 7 SPST adder

The SPST has a detection logic circuit find out if a transition in data bits of the resultwill occur in circuits, e.g., multipliers or adders. When a part of the data doesn’t cause any change in the final result of the circuit, that portion of the data is latched to avoid unwanted transitions inside the processing units.

2.2.8 Comparison Between Different Types Of Adders:

Table 3 Comparison between different types of Adders

S.No	Adder Type	No.Of AND Gates	No.Of EX-OR Gates	No.Of OR Gates
1	Half-Adder	1	1	-
2	Full Adder	2	2	1
3	8-Bit Ripple Carry Adder	16	16	8
4	8-Bit Carry – Look Ahead Adder	16	16	8
5	4-Bit Carry Save Adder	16	16	8
6	4-Bit Carry Select Adder	16	16	8

2.3 MULTIPLIERS

Today’s processors require a very high-speed operation. Arithmetic operations such as addition, subtraction and multiplication are used in various digital circuits for high-speed computation. Multiplication is the basic arithmetic operation in signal processing. All the signal and data processing operations like digital signal processing contain multiplication.

Speed is an essential parameter in a multiplication operation. It can be increased by reducing the number of steps in the computation process. In a digital system design, the parameters that determine the performance of the system are speed, power and area. As the multiplier requires the longest delay among the basic operational blocks in a digital system, the critical path is determined more by the multiplier. Also, a multiplier consumesmuch area and dissipates more power. Hence, designing multipliers which offer a combination of the above parameters is better.

A multiplier is one of the key hardware blocks in many digital signal processing systems. Some of the DSP applications where a multiplier plays an important roleinclude digital filters, digital communications and spectral analysis. Many current DSP applications are targeted at portable, battery-operated systems, in order that power dissipation becomes one among the first design constraints. As multipliers are complex circuits and have to operate at a high system clock rate, reducing the delayof a multiplier is an important a part of satisfying the overall design. This operation involves two major steps: Partial product generation and accumulation.

2.3.1 PARTIAL PRODUCTS

Formation of partial products

The basic algorithm for multiplication of two binary numbers, M(multiplier) and N(multiplicand) makes use of the distributive property of multiplication. That is, if M canbe written as a sum of smaller numbers

$$M.N = (M_0+M_1+\ldots\ldots\ldots +M_{m-1}).\ N = M_0N+M_1N+\ldots\ldots\ldots\ldots+M_{m-1}N$$

Also, a multiplier consumes most of the area and dissipates more power. Hence designing multipliers which offer either of the following design targets – high speed, low power consumption, less area or even a combination of them is preferred.

2.3.2 TYPES OF MULTIPLIERS

a. Shift-and-Add Multiplication

In this method, we add a number with itself and rotate the other number each timeand shift it by one bit to left along with the carry. If carry is present add those two numbers.

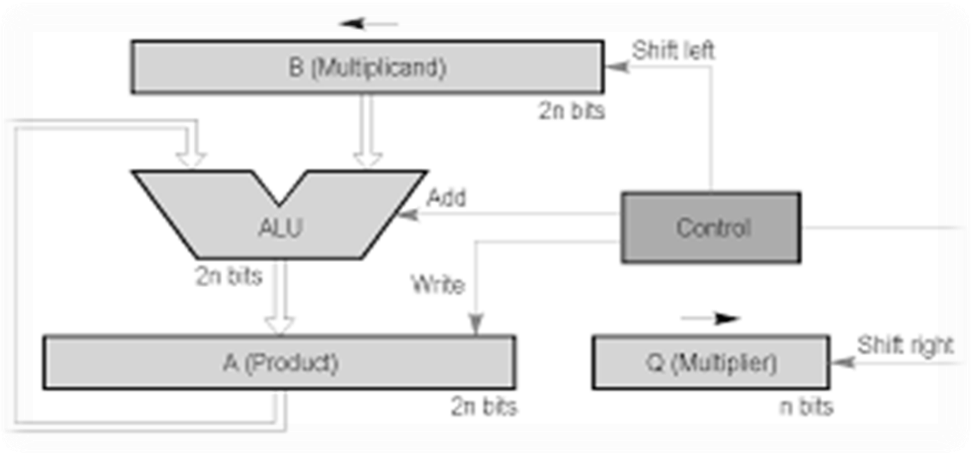


Fig 8 Shift- and add multiplier

This algorithm adds the multiplicand to itself by M times, where M denotes the multiplier. To multiply these two numbers this
algorithm takes the digits of the multiplier and places the intermediate product in the appropriate position to the left of earlier results.

CHAPTER 3
CANONICAL SIGNED DIGIT

CSD representations have proven to be useful in implementating multipliers with reduced complexity, because cost of multiplication is a direct function of non zero bits in the multiplier and as CSD algorithm helps in reducing the number of these non zero bits it is very useful in implementing efficient multiplier.

The CSD format aims to scale back the amount of additives during multiplication. The CSD format features a ternary set as against a binary set-in number representation. The symbols utilized in this format are {-1, 0, 1}. The goal is to group consecutive 1s andalter them to a ternary representation from binary representation. This is done ranging from the rightmost 1 and proceeding left until the last 1. So, this never has adjacent non- zero bits. It is proved that the number of operations never exceeds n/2 and on a mean, it are often reduced to n/3.

3.1 Canonical Signed Digit Algorithm

Conversion from a binary representation to CSD representation requires the following steps:

- Observe where there are two consecutive 1's and convert the right most 1 into -1
- Add +1 to the next bits

The CSD presentation of a number is unique. The number of nonzero digits is minimal. There cannot be two consecutive non-zero digits

for example, the binary value 1 1 1 1 1 (decimal number 31) could be written as the

signed-digit value 1 0 0 0 0 -1 = 2^5 - 2^0 =d31

CSD representation of integers 1, 2, … 10 is as follows:

Table 4 Binary to CSD conversion

B2	B1	B0	C3	C2	C1	C0
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	0	-1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	1	0	-1	0
1	1	1	1	0	0	-1

Converting binary number into CSD number can be achieved by continuously comparing adjacent two bits from the LSB to MSB. And to represent one bit in the CSD representation require two binary bits.

So, -1 will be represented with 11. Here MSB represents sign bit and LSB represents main bit.

If the sign bit is 1;

Then it is a negative number

Else;

It is a positive number. i.e., sign bit ==0

And the main bit represents magnitude of the CSD bit.

As the conversion process needs to compare present bit and next b it of the binary number and also the carry of the previous comparison as this generated carry also makes impact on the present bit of CSD number.

The truth table for this conversion which consists of present and next bit of binary number And previous carry as inputs and sign and main bits of CSD number and present carry as output is as follows:

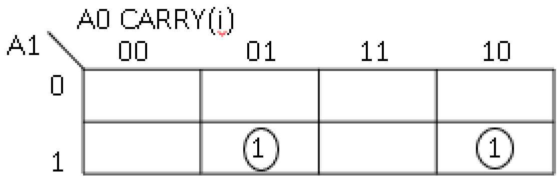
If the input is 4 bit : A3 A2 A1 A0

Table 5 Binary to CSD conv. Truth Table

A1	**A0**	**C(i)**	**sign**	**main**	**C(i+1)**
0	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**	**0**
0	**1**	**0**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**	**1**
1	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**1**	**1**	**1**
1	**1**	**0**	**1**	**1**	**1**
1	**1**	**1**	**0**	**0**	**1**

Same truth table works for remaining bit comparisons. By using above truth table and k-map reduction technique calculating the Boolean expressions for sign bit, main bit and present carry.

DERIVATIONS FROM TRUTH TABLE
SIGN:

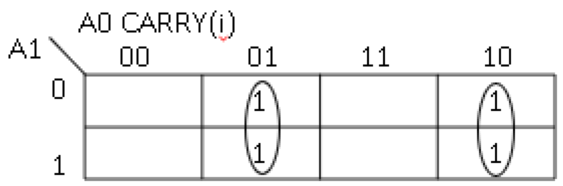


⇨ A1.A0'.Carry(i)+A1.A0.Carry(i)'

⇨ A1(A0'.Carry(i)+A0.Carry(i)'

Sign =A1(A0 ^ C(i)).

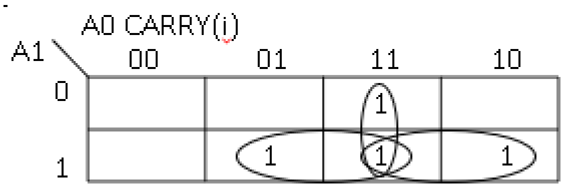
MAIN:



⇨ A0’.Carry(i)+A0.Carry(i)’

Main=A0 ^ C(i).

C(i+1):



C(i+1) =A0.C(i)+A1.C(i)+A1.A0.

These Boolean expressions are used to form a circuit called CSD converter circuit. This circuit consists of Two adjacent bits of binary number as inputs along with previous carry. And outputs of this circuit will be sign, main bits of CSD number and present carry which will be carried forward to next comparison.

If A0 and A1 are adjacent bits to be compared and C0 is the previous carry and om0 and os0 are main and sign bits of CSD number and c1 is the present carry then the CSD converter circuit is as follows:

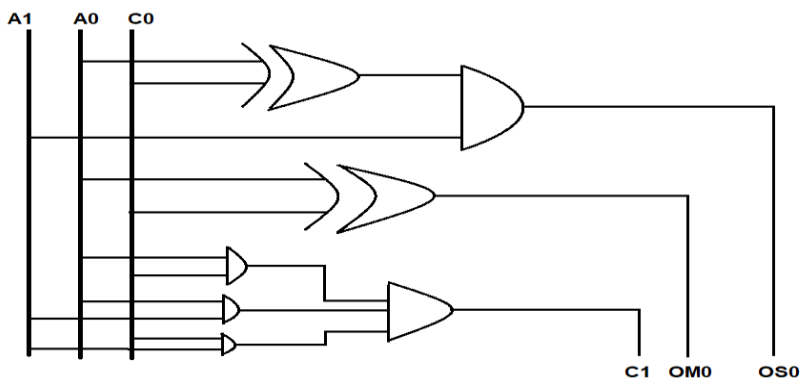


FIG 9 CSD Converter Circuit

Now to convert given entire binary number into CSD number this CSD converter circuit will be used repeatedly.
If the input is A= A3 A2 A1 A0
And outputs:

Main = om4 om3 om2 om1 om0
Sign = os4 os3 os2 os1 os0
And always the first previous carry will be taken as 0. i.e., c0=0.
The block diagram for binary to CSD converter is as follows:

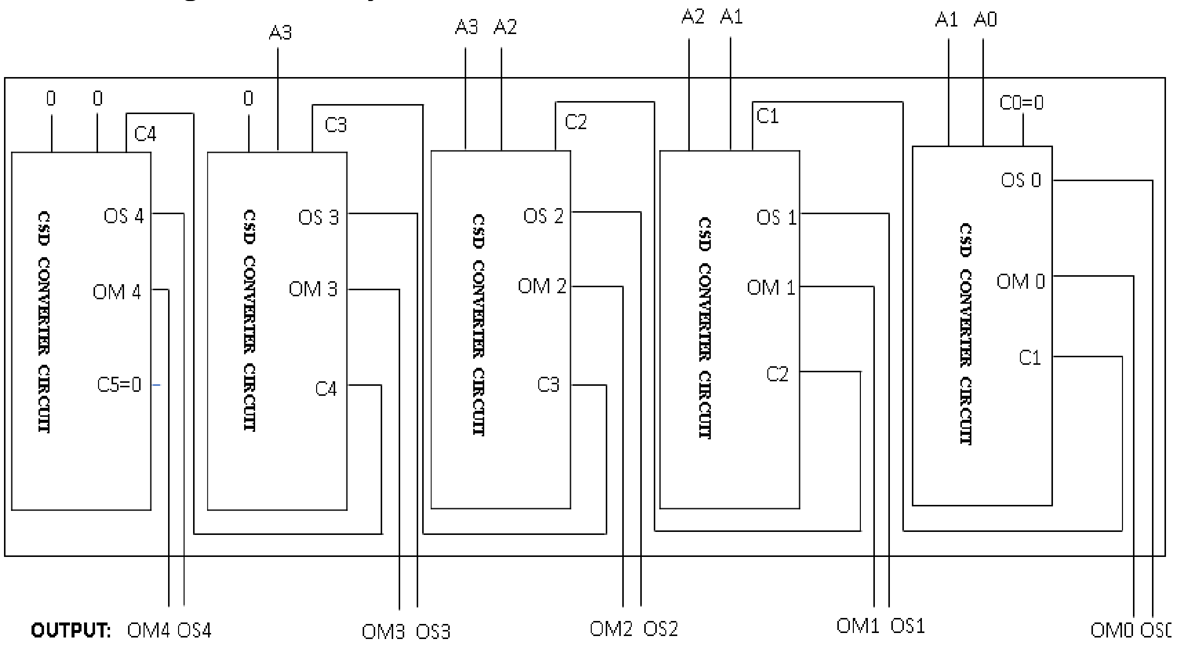


FIG 10 Binary to CSD conv. Block Diagram

3.2 Comparison of Binary multiplication Vs. CSD multiplication

Let us consider an example-14 multiplied with 15.

Multiplicand => 1110; Multiplier=> 1111.

Binary Multiplication

1110*1111

1110
1110x
1110xx
1110xxx

11010010

CSD Multiplication

CSD code for multiplier-1000-1
1110*1000-1

-1-1-10
1110 x x x x

1110-1-1-10

2^7+2^6+2^4+2^1=d210 (2^7+2^6+2^5)-(2^3+2^2+2^1)=d210

Here when we observe binary multiplication the number of stages involved for multiplication are more when compared to that of the stages of CSD multiplications. It is clearly observed that the number of stages are decreased as the number of 1’s of the multiplier are reduced and are converted into 0’s using the CSD algorithm. Later after performing the multiplication in binary and CSD respectively the result is converted into decimal format. And when observed the results both are of same value in decimal format. That’s the reason we are using CSD algorithm for efficient multiplication- as the number of stages or partial products terms are reduced the hardware requirement is also reduced correspondingly which leads to reduction in area utilization.

3.3 CSD FLOW

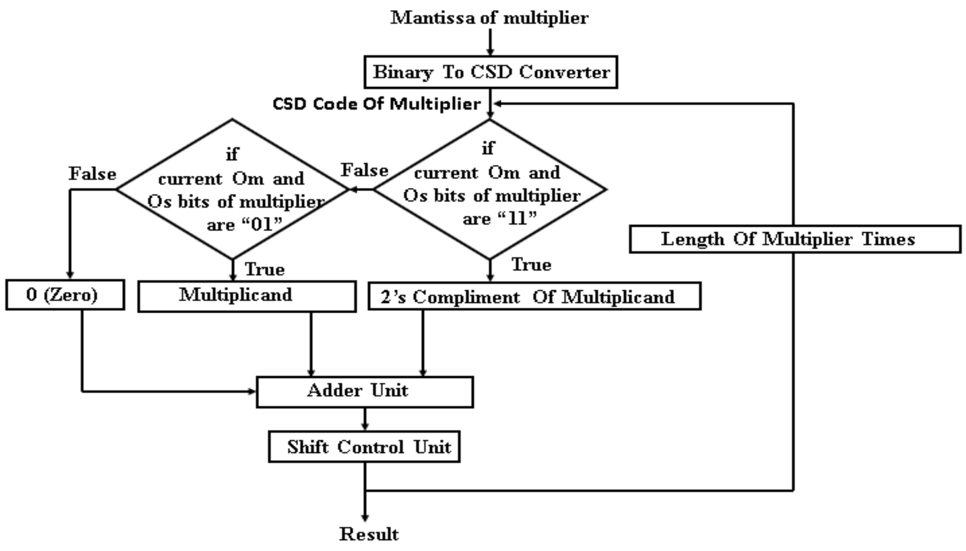

Mantissa of multiplier
Binary To CSD Converter
CSD Code Of Multiplier
if current Om and Os bits of multiplier are “01”
False
False
if current Om and Os bits of multiplier are “11”
Length Of Multiplier Times
True
True
0 (Zero)
Multiplicand
2’s Compliment Of Multiplicand
Adder Unit
Shift Control Unit
Result

FIG 11 CSD Multiplication flow chart

3.4 FPM Using CSD

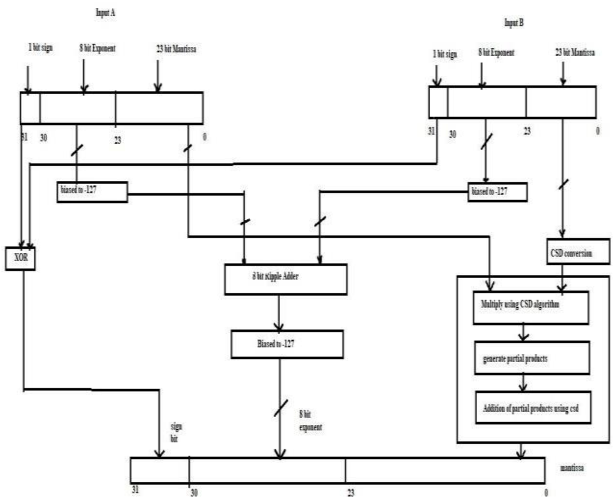


FIG 12 FPM Using CSD

CHAPTER 4
OVERVIEW OF FPGA AND EDA SOFTWARE

4.1 INTRODUCTION

Developing a large FPGA –based system is an involved process that consists of many complex transformations and optimization algorithms. Software tools are needed to automate some of the tasks.

We use basys 3 Board which is a complete, ready-to- use digital circuit development platform based on the latest Artix-7 Field Programmable Gate Array (FPGA) (XC7A35T- 1CPG236C) from Xilinx for synthesis and implementation, and use the Vivado Design Suite for simulation.

A Field Programmable Gate Array (FPGA) is a logic device that contains a two-dimensional add shift of generic logic cells and programmable switches. A logic cell can be programmed to perform a simple function, and a programmable switch can be customized to provide interconnection among the logic cells.

A custom design can be implemented by specifying the function of each logic cell and selectively setting the connection of each programmable switch. Once the design and synthesis are completed, we can use a simple adapter cable to download the desired logic cell and switch configuration to the FPGA device and obtain the custom circuit. Since this process can be done “in the field” rather than “in fabrication facility (fab),” the device is known as field programmable.

4.2 OVERVIEW OF DIGILENT BASYS 3 BOARD

The Basys 3 board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7 Field Programmable Gate Array (FPGA) from Xilinx®. With its high-capacity FPGA (Xilinx part number XC7A35T- 1CPG236C), low overall cost, and collection of USB, VGA, and other ports, the Basys 3 can host designs ranging from introductory combinational circuits to complex sequential circuits like embedded processors and controllers. It includes enough switches, LEDs, and other I/O devices to allow a large number of designs to be completed without the need for any additional hardware, and enough uncommitted FPGA I/O pins to allow designs to be expanded using Digilent Pmods or other custom boards and circuits.

4.2.1 Features Of Basys 3

- 33,280 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops)
- 1,800 Kbits of fast block RAM
- Five clock management tiles, each with a phase-locked loop(PLL)
- 90 DSP slices
- Internal clock speeds exceeding 450MHz
- On-chip analog-to-digital converter(XADC)
- 16 user switches
- 16 user LEDs
- 5 user push buttons
- 4-digit7-segmentdisplay
- Three Pmod ports
- Pmod for XADC signals
- 12-bit VGA output
- USB-UART Bridge
- Serial Flash
- Digilent USB-JTAG port for FPGA programming and communication
- USB HID Host for mice, keyboards and memory sticks

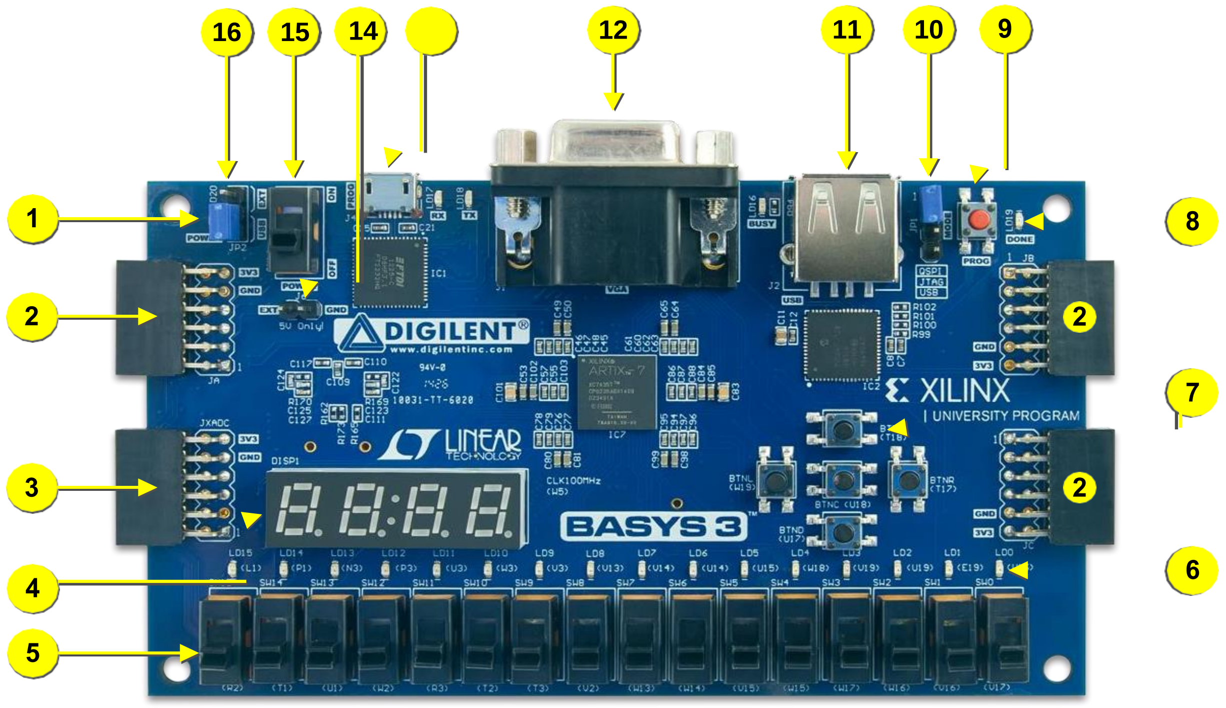


Figure13 Basys3FPGAboardwithcallouts.

Table 6 Basys 3 FPGA Component Description

Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod port(s)	10	Programming mode jumper
3	Analog signal Pmod port (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power Switch
8	FPGA programming done LED	16	Power Select Jumper

4.2.2 Power Supplies

The Basys 3 board can receive power from the Digilent USB-JTAG port (J4) or from a 5V external power supply. Jumper JP3 (near the power switch) determines which source is used. All Basys 3 power supplies can be turned on and off by a single logic-level power switch (SW16). A power-good LED (LD20), driven by the "power good" output of the LTC3633 supply, indicates that the supplies are turned on and operating normally. An overview of the Basys 3 power circuit is shown in Fig. 2.

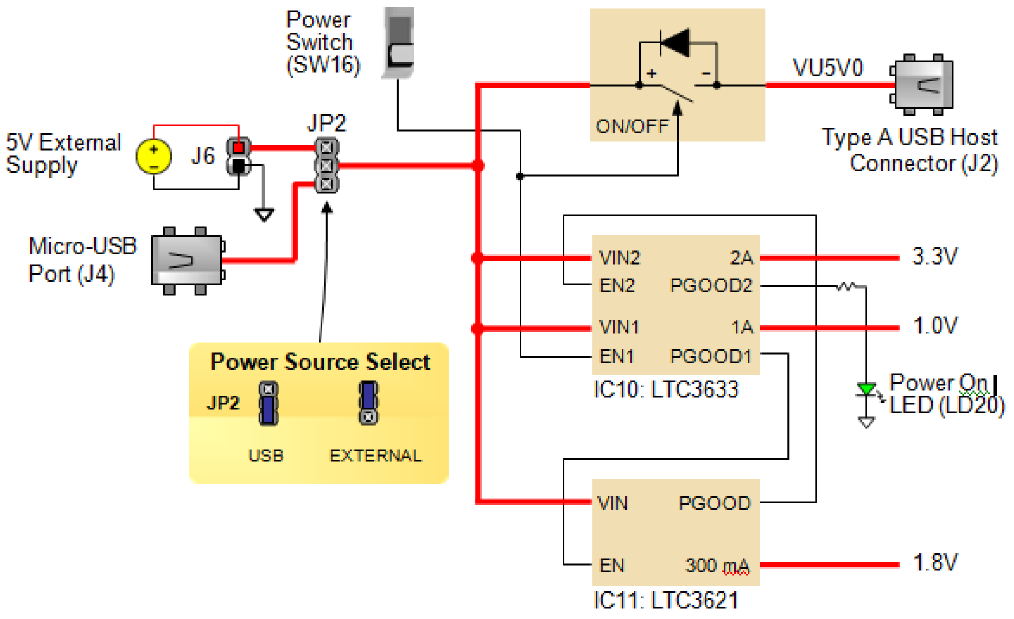


Figure 14 Basys 3 power circuit.

The USB port can deliver enough power for the vast majority of designs. A few demanding applications, including any that drive multiple peripheral boards, might require more power than the USB port can provide. Also, some applications may need to run without being connected to a PC's USB port. In these instances an external power supply or battery pack can be used.

An external power supply can be used by plugging into the external power header (J6) and setting jumper JP2 to "EXT". The supply must deliver 4.5VDC to 5.5VDC and at least 1A of current (i.e., at least 5W of power). Many suitable supplies can be purchased through Digi-Key or other catalog vendors.

An external battery pack can be used by connecting the battery's positive terminal to the "EXT" pin of J6 and the negative terminal to the "GND" pin of J6. The power provided to USB devices that are connected to Host connector J2 is not regulated. Therefore, it is necessary to limit the maximum voltage of an external battery pack to 5.5V DC. The minimum voltage of the battery pack depends on the application; if the USB Host function (J2) is used, at least 4.6V needs to be provided. In other cases, the minimum voltage is 3.6V.

Voltage regulator circuits from Linear Technology create the required 3.3V, 1.8V, and 1.0V supplies from the main power input. Table 2 provides additional information (typical currents depend strongly on FPGA configuration and the values provided are typical of medium size/speed designs).

Table 7 Basys 3 power supplies.

Supply	Circuits	Device	Current (max/typical)
3.3V	FPGA I/O, USB ports, Clocks, Flash, PMODs	IC10: LTC3633	2A/0.1 to 1.5A
1.0V	FPGA Core	IC10: LTC3633	2A/ 0.2 to 1.3A
1.8V	FPGA Auxiliary and Ram	IC11: LTC3621	300mA/ 0.05 to 0.15A

4.2.3 FPGA Configuration

After power-on, the Artix-7 FPGA must be configured (or programmed) before it can perform any functions. You can configure the FPGA in one of three ways:

A PC can use the Digilent USB-JTAG circuitry (port J4, labeled "PROG") to program the FPGA any time the power is on.

A file stored in the nonvolatile serial (SPI) flash device can be transferred to the FPGA using the SPI port.

A programming file can be transferred from a USB memory stick attached to the USB HID port.

Figure 3 shows the different options available for configuring the FPGA. An on-board "mode" jumper (JP1) selects between the programming modes.

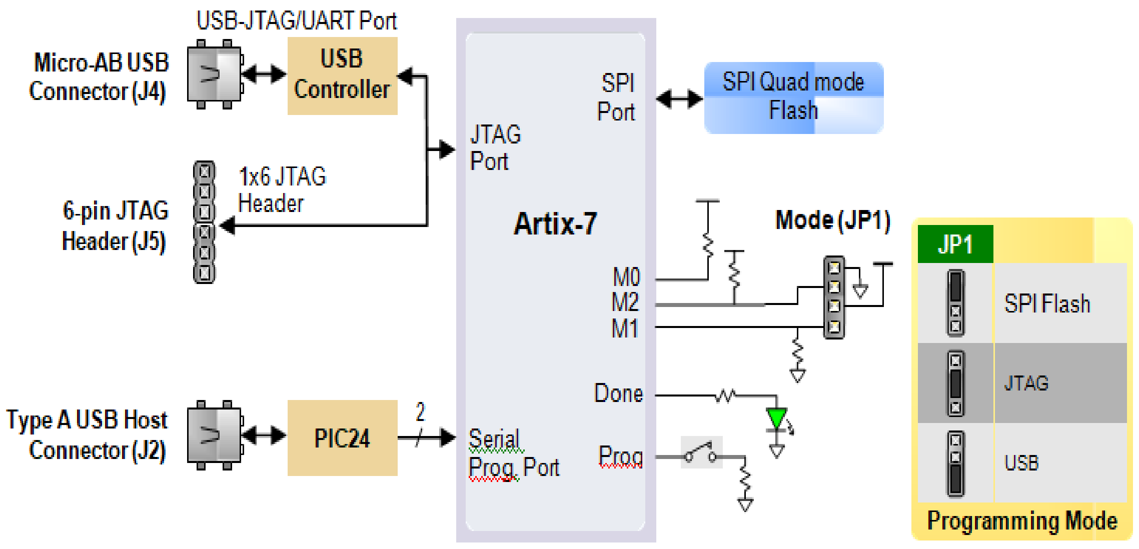


Figure 15 Basys 3 configuration options

The FPGA configuration data is stored in files called bitstreams that have the .bit file extension. The Vivado software from Xilinx can create bitstreams from VHDL, Verilog®, or schematic-based source files.

Bitstreams are stored in SRAM-based memory cells within the FPGA. This data defines the FPGA's logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

An Artix-7 35T bitstream is typically 17,536,096 bits and can take a long time to transfer. The time it takes to program the Basys 3 can be decreased by compressing the bitstream before programming, and then allowing the FPGA to decompress the bitstream itself during configuration. Depending on design complexity, compression ratios of 10x can be achieved. Bitstream compression can be enabled within the Xilinx Tools (Vivado) to occur during generation. For instructions on how to do this, consult the Xilinx documentation for the toolset being used.

After being successfully programmed, the FPGA will cause the "DONE" LED to illuminate. Pressing the "PROG" button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from whatever method has been selected by the programming mode jumper.

The following sections provide greater detail about programming the Basys 3 using the different methods available.

4.2.3.1 JTAG Programming

The Xilinx Tools typically communicate with FPGAs using the Test Access Port and Boundary-Scan Architecture, commonly referred to as JTAG. During JTAG programming, a .bit file is transferred from the PC to the FPGA using the onboard Digilent USB-JTAG circuitry (port J4) or an external JTAG programmer, such as the Digilent JTAG-HS2attached to port J5 (located below port JA). You can perform JTAG programming any time after the Basys 3 has been powered on regardless of what the mode jumper (JP1) is set to. If the FPGA is already configured, then the existing configuration is overwritten with the bitstream being transmitted over JTAG. Setting the mode jumper tothe JTAG setting (seen in Fig. 3) is useful to prevent the FPGA from being configured from any other bitstream source until a JTAG programming occurs.

Programming the Basys 3 with an uncompressed bitstream using the on-board USB_JTAG circuitry usually takes around five seconds. JTAG programming can be done using the hardware server in Vivado. The demonstration project available at digilentinc.com provides an in-depth tutorial on how to program your board.

4.2.3.2 JTA Programming

When programming a nonvolatile flash device, a bitstream file is transferred to the flash in a two-step process. First, the FPGA is programmed with a circuit that can program flash devices, and then data is transferred to the flash device via the FPGA circuit (this complexity is hidden from the user by the Xilinx Tools). After the flash device has been programmed, it can automatically configure the FPGA at a subsequent power-on or reset event as determined by the mode jumper setting (see Fig. 3). Programming files stored in the flash device will remain until they are overwritten, regardless of power-cycle events.

Programming the flash can take as long as one or two minutes, which is mostly due to the lengthy erase process inherent to the memory technology. Once written, however, FPGA configuration can be very fast – less than a second. Bitstream compression, SPI bus width, and configuration rate are factors controlled by the Xilinx Tools thatcan affect configuration speed.

Quad-SPI programming can be performed using Vivado.

4.2.3.3 USB Host Programming

You can program the FPGA from a pen drive attached to the USB-HID port (J2) by doing the following:

1. Format the storage device (Pen drive) with a FAT32 file system.

2. Place a single bit configuration file in the root directory of the storage device.
3. Attach the storage device to the Basys 3.
4. Set the JP1 Programming Mode jumper on the Basys 3 to "USB".
5. Push the PROG button or power-cycle the Basys 3.

The FPGA will automatically be configured with the .bit file on the selected storage device. Any .bit files that arenot built for the proper Artix-7 device will be rejected by the FPGA.

The Auxiliary Function Status, or "BUSY" LED (LD16), gives visual feedback on the state of the configuration processwhen the FPGA is not yet programmed:

- When steadily lit, the auxiliary microcontroller is either booting up or currently reading the configurationmedium (pen drive) and downloading a bitstream to the FPGA.
- A slow pulse means the microcontroller is waiting for a configuration medium to be plugged in.
- In case of an error during configuration, the LED will blink rapidly

When the FPGA has been successfully configured, the behavior of the LED is application-specific. For example, if a USB keyboard is plugged in, a rapid blink will signal the receipt of an HID input report from the keyboard.

4.2.4 Memory

The Basys 3 board contains a 32Mbit non-volatile serial Flash device, which is attached to the Artix-7 FPGA using a dedicated quad-mode (x4) SPI bus. The connections and pin assignments between the FPGA and the serial flash device are shown in Fig. 4.

FPGA configuration files can be written to the Quad SPI Flash (Spansion part number S25FL032), and mode settings are available to cause the FPGA to automatically read a configuration from this device at power on. An Artix-7 35T configuration file requires just over two Mbytes of memory, leaving approximately 48% of the flash device available for user data.

NOTE: Refer to the manufacturer's data sheets and the reference designs posted on Digilent's website for moreinformation about the memory devices.

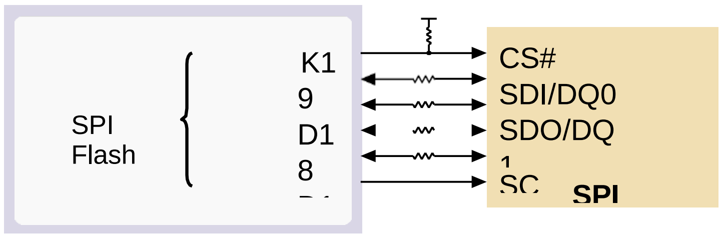


Figure 16 Basys 3 external memory

4.2.5 Oscillators/Clocks

The Basys 3 board includes a single 100 MHz oscillator connected to pin W5 (W5 is a MRCC input on bank 34). The input clock can drive MMCMs or PLLs to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design. Some rules restrict which MMCMs and PLLs may be driven by the 100 MHz input clock. For a full description of these rules and of the capabilities of the Artix-7 clocking resources, refer to the "7 Series FPGAs Clocking Resources User Guide" available from Xilinx.

Xilinx offers the LogiCORE™ Clocking Wizard IP to help users generate the different clocks required for a specific design. This wizard properly instantiates the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy to use wrapper component around these clocking resources that can be inserted into the user's design. The Clocking Wizard can be accessed from within IP Catalog, which can be found under the Project Manager section of the Flow Navigator in Vivado.

4.2.6 USB-UART Bridge(Serial Port)

The Basys 3 includes an FTDI FT2232HQ USB-UART bridge (attached to connector J4) that allows you to use PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the "Virtual Com Port" or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the B18 and A18 FPGA pins.

Two on-board status LEDs provide visual feedback on traffic flowing through the port: the transmit LED (LD18) and the receive LED (LD17). Signal names that imply direction are from the point-of-view of the DTE (Data Terminal Equipment), in this case the PC.

The FT2232HQ is also used as the controller for the Digilent USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the Basys 3 to be programmed, communicated with via UART, and powered from a computer attached with a single Micro USB cable. The connections between the FT2232HQ and the Artix-7 are shown in Fig. 17.

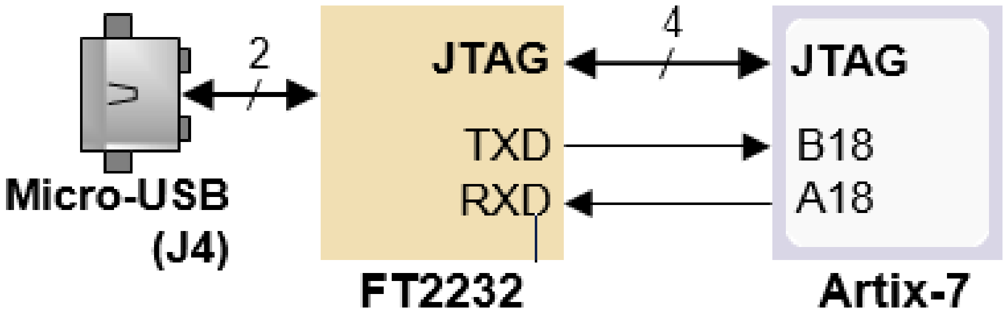


Figure 17 basys3 FT2232HQ Connection

4.2.7 USB HID Host

The Auxiliary Function microcontroller (Microchip PIC24FJ128) provides the Basys 3 with USB HID host capability. After power-up, the microcontroller is in configuration mode, either downloading a bitstream to the FPGA or waiting for it to be programmed from other sources. Once the FPGA is programmed, the microcontroller switches to application mode, which in this case is USB HID Host mode. Firmware in the microcontroller can drive a mouse or a keyboard attached to the type A USB connector at J2 labeled "USB." Hub support is not currently available, so only a single mouse or a single keyboard can be used. The PIC24 drives several signals into the FPGA – two are used to implement a standard PS/2 interface for communication with a mouse or keyboard, and the others are connected to the FPGA's two-wire serial programming port, so the FPGA can be programmed from a file stored on a USB pen drive.

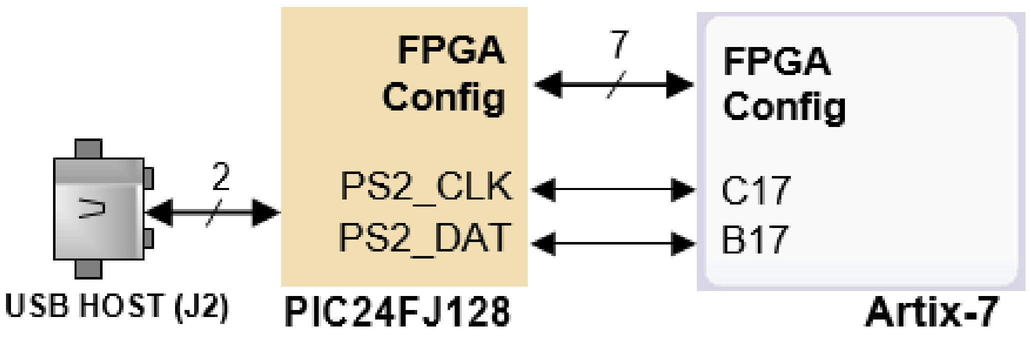
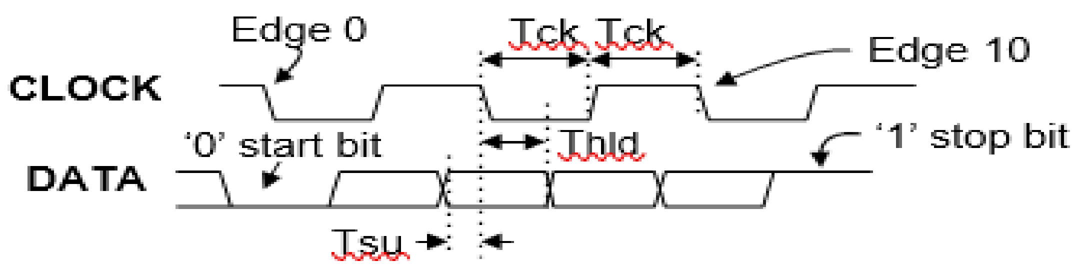


Figure 18 Basys 3 PIC24 connections.

4.2.7.1 HID CONTROLLER

The Auxiliary Function microcontroller hides the USB HID protocol from the FPGA and emulates an old-style PS/2 bus. The microcontroller behaves just like a PS/2 keyboard or mouse would. This means new designs can re-use existing PS/2 IP cores. Mice and keyboards that use the PS/2 protocol use a two-wire serial bus (clock and data) to communicate with a host. On the Basys 3, the microcontroller emulates a PS/2 device while the FPGA plays the role of the host. Both the mouse and the keyboard use 11-bit words that include a start bit, data byte (LSB first), odd parity, and stop bit, but the data packets are organized differently, and the keyboard interface allows bi- directional data transfers (so the host device can illuminate state LEDs on the keyboard). Bus timings are shown in Fig. 8.



Symbol	Parameter	Min	Max
T_{CK}	Clock time	30us	50us
T_{SU}	Data-to-clock setup time	5us	25us
T_{HLD}	Clock-to-data hold time	5us	25us

Figure 19 PS/2 device-to host timing diagram.

The clock and data signals are only driven when data transfers occur; otherwise they are held in the idle state at logic '1.' This requires that when the PS/2 signals are used in a design, internal pull-ups must be enabled in the FPGA on the data and clock pins. The clock signal is normally driven by the device, but may be held low by the host in special cases. The timings define signal requirements for mouse-to-host communications and bi-directional keyboard communications. A PS/2 interface circuit can be implemented in the FPGA to create a keyboard or mouse interface.

When a keyboard or mouse is connected to the Basys 3, a "self-test passed" command (0xAA) is sent to the host. After this, commands may be issued to the device. Since both the keyboard and the mouse use the same PS/2 port, one can tell the type of device connected using the device ID. This ID can be read by issuing a Read ID command (0xF2). Also, a mouse sends its ID (0x00) right after the "self-test passed" command, which distinguishes it from a keyboard.

4.2.7.2 Keyboard

The keyboard uses open-collector drivers so the keyboard, or an attached host device, can drive the two-wire bus(if the host device will not send data to the keyboard, then the host can use input-only ports).

PS/2-style keyboards use scan codes to communicate key press data. Each key is assigned a code that is sent whenever the key is pressed. If the key is held down, the scan code will be sent repeatedly about once every 100ms. When a key is released, an F0 key-up code is sent, followed by the scan code of the released key. If a key can be shifted to produce a new character (like a capital letter), then a shift character is sent in addition to the scancode and the host must determine which ASCII character to use. Some keys, called extended keys, send an E0 ahead of the scan code (and they may send more than one scan code). When an extended key is released, an E0 F0key-up code is sent, followed by the scan code. Scan codes for most keys are shown in Fig. 9.

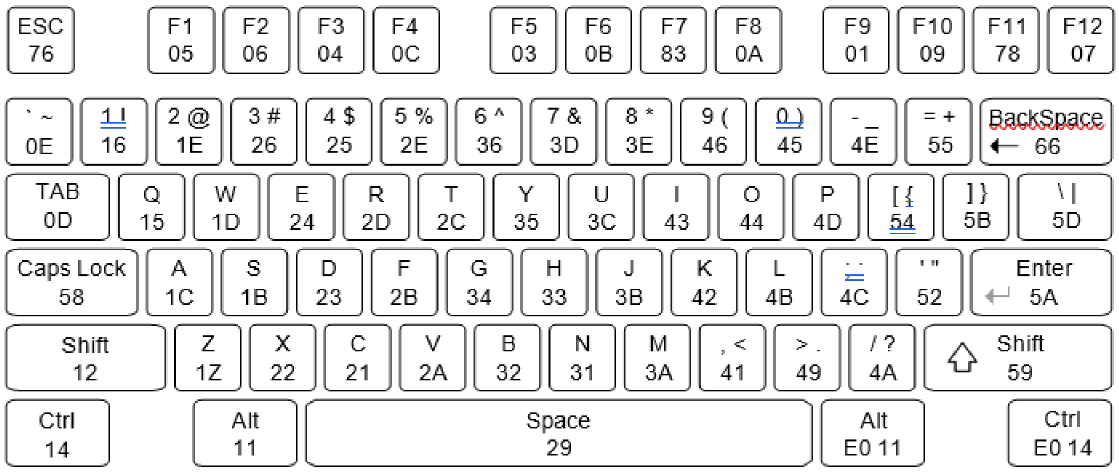


Figure 20 Keyboard scan codes.

A host device can also send data to the keyboard. Table 3 shows a list of some common commands a host mightsend.

The keyboard can send data to the host only when both the data and clock lines are high (or idle). Because the host is the bus master, the keyboard must check to see whether the host is sending data before driving the bus. To facilitate this, the clock line is used as a "clear to send" signal. If the host drives the clock line low, the keyboard must not send any data until the clock is released. The keyboard sends data to the host in 11-bit words that contain a '0' start bit, followed by 8-bits of scan code (LSB first), followed by an odd parity bit, and terminated witha '1' stop bit. The keyboard generates 11 clock transitions (at 20 to 30 KHz) when the data is sent, and data is valid on the falling edge of the clock.

Table 8 Keyboard commands.

Command	Action
ED	Set Num Lock, Caps Lock, and Scroll Lock LEDs. Keyboard returns FA after receiving ED, then host sends a byte to set LED status: bit 0 sets Scroll Lock, bit 1 sets Num Lock, and bit 2 setsCaps lock. Bits 3 to 7 are ignored.
EE	Echo (test). Keyboard returns EE after receiving EE.
F3	Set scan code repeat rate. Keyboard returns F3 on receiving FA, then host sends second byte to set the repeat rate.
FE	Resend. FE directs keyboard to re-send most recent scan code.
FF	Reset. Resets the keyboard.

4.2.7.3 MOUSE

Once entered in stream mode and data reporting has been enabled, the mouse outputs a clock and data signal when it is moved. Otherwise, these signals remain at logic '1.' Each time the mouse is moved, three 11-bit words are sent from the mouse to the host device, as shown in Fig. 10. Each of the 11-bit words contains a '0' start bit, followed by 8 bits of data (LSB first), followed by an odd parity bit, and terminated with a '1' stop bit. Thus, each data transmission contains 33 bits, where bits 0, 11, and 22 are '0' start bits, and bits 11, 21, and 33 are '1' stop bits. The three 8-bit data fields contain movement data as shown in the Fig. 10. Data is valid at the falling edge ofthe clock, and the clock period is 20 to 30 KHz.

The mouse assumes a relative coordinate system wherein moving the mouse to the right generates a positive number in the X field, and moving to the left generates a negative number. Likewise, moving the mouse up generates a positive number in the Y field, and moving down represents a negative number (the XS and YS bits in the status byte are the sign bits – a '1' indicates a negative number). The magnitude of the X and Y numbers represent the rate of mouse movement; the larger the number, the faster the mouse is moving (the XV and YV bits in the status byte are movement overflow indicators – a '1' means overflow has occurred). If the mouse movescontinuously, the 33-bit transmissions are repeated every 50ms or so. The L and R fields in the status byte indicateLeft and Right button presses (a '1' indicates that the button is being pressed).

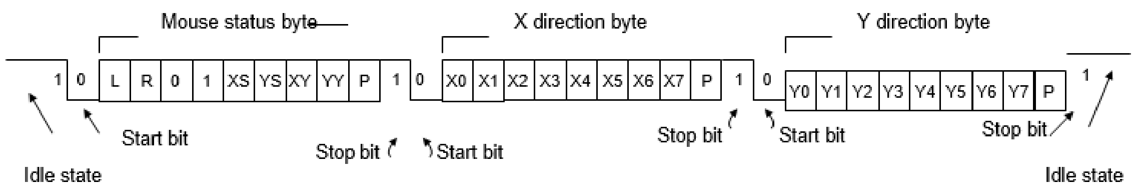


Figure 21 Mouse data format

The microcontroller also supports Microsoft® IntelliMouse®-type extensions for reporting back a third axisrepresenting the mouse wheel, as shown in Table 4.

Table 9 Microsoft Intellimouse-type extensions, commands, and actions.

Command	Action
EA	Set stream mode. The mouse responds with "acknowledge" (0xFA) then resets its movement counters and enters stream mode.
F4	Enable data reporting. The mouse responds with "acknowledge" (0xFA) then enables data reporting and resets its movement counters. This command only affects behavior in streammode. Once issued, mouse movement will automatically generate a data packet.
F5	Disable data reporting. The mouse responds with "acknowledge" (0xFA) then disables data reporting and resets its movement counters.
F3	Set mouse sample rate. The mouse responds with "acknowledge" (0xFA) then reads one morebyte from the host. This byte is then saved as the new sample rate, and a new "acknowledge" packet is issued.
FE	Resend. FE directs mouse to re-send last packet.
FF	Reset. The mouse responds with "acknowledge" (0xFA) then enters reset mode.

4.2.8 VGA PORT

NOTE: A helpful way to understand the way that VGA signals are transmitted is to understand the method of whichCRT (Cathode Ray Tubes) function for displaying images. Although the technology may seem outdated, it is from this legacy that many of the signal names and timings have originated.

The Basys 3 board uses 14 FPGA signals to create a VGA port with 4-bits per colour and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The colour signals use resistor-divider circuits that work in conjunction with the 75-ohm termination resistance of the VGA display to create 16 signal levels each on the red, green, and blue VGA signals. This circuit, shown in Fig. 11, produces video colour signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 4096 different colours can be displayed, one for each unique 12-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and colour signals with the correct timing in order to produce a working display system.

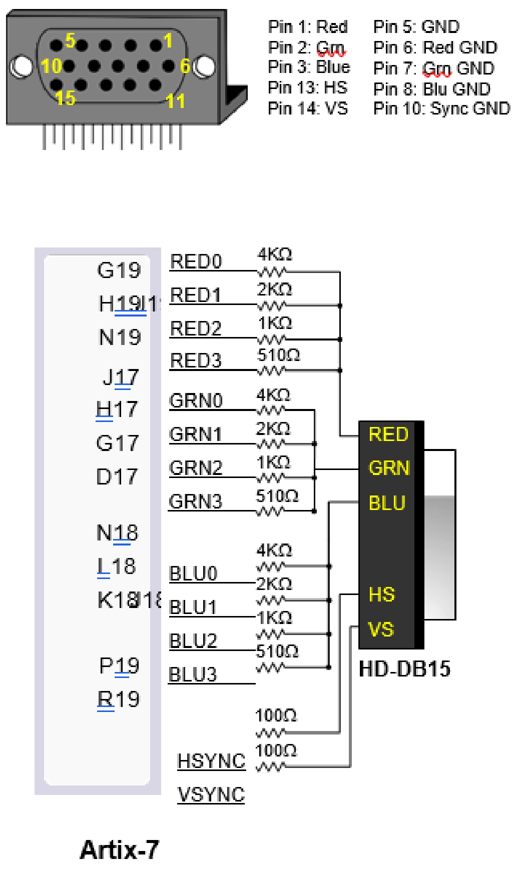


FIG 22 VGA Port Pin Description.

4.2.8.1 VGA SYSTEM TIMING

VGA signal timings are specified, published, copyrighted, and sold by the VESA® organization (www.vesa.org). The following VGA system timing information is provided as an example of how a VGA monitor might be driven in 640 by 480 mode.

NOTE: For more precise information, or for information on other VGA frequencies, refer to documentation available at the VESA website.

CRT-based VGA displays use amplitude-modulated moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permittivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the same signal timings as CRT displays (so the "signals" discussion below pertains to both CRTs and LCDs). Color CRT displays use three electron beams (one for red, one for blue, and one for green) to energize the phosphor that coats the inner side of the display end of a cathode ray tube (see Fig. 12).

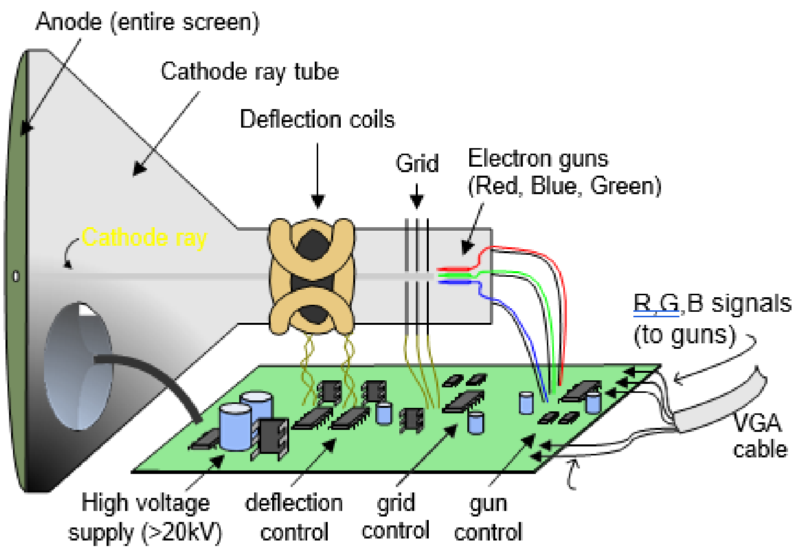
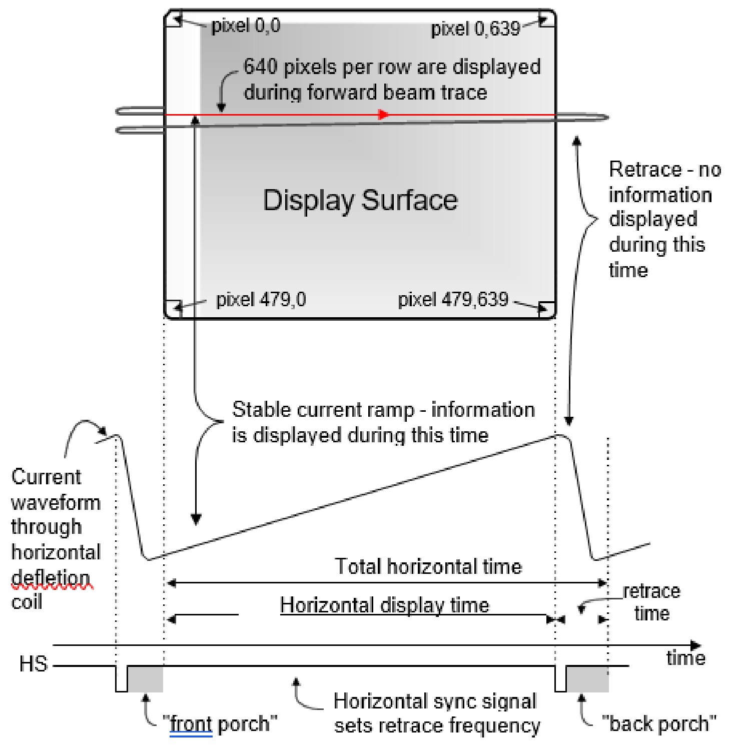


Figure 23 Colour CRT display.

Electron beams emanate from "electron guns" which are finely-pointed heated cathodes placed in close proximity to a positively charged annular plate called a "grid." The electrostatic force imposed by the grid pulls rays of energized electrons from the cathodes, and those rays are fed by the current that flows into the cathodes. These particle rays are initially accelerated towards the grid, but they soon fall under the influence of the much larger electrostatic force that results from the entire phosphor-coated display surface of the CRT being charged to 20kV (or more). The rays are focused to a fine beam as they pass through the center of the grids, and then they accelerate to impact on the phosphor-coated display surface. The phosphor surface glows brightly at the impact point, and it continues to glow for several hundred microseconds after the beam is removed. The larger the current fed into the cathode, the brighter the phosphor will glow.

Between the grid and the display surface, the beam passes through the neck of the CRT where two coils of wire produce orthogonal electromagnetic fields. Because cathode rays are composed of charged particles (electrons), they can be deflected by these magnetic fields. Current waveforms are passed through the coils to produce magnetic fields that interact with the cathode rays and cause them to transverse the display surface in a "raster" pattern, horizontally from left to right and vertically from top to bottom, as shown in Fig. 13. As the cathode ray moves over the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the display at the cathode ray impact point. Information is only displayed when the beam is moving in the "forward" direction (left to right and top to bottom), and not during the time the beam is reset back to the left or top edge of the display. Much of the potential display time is therefore lost in "blanking" periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass. The size of the beams, the frequency at which the beam can be traced across the display, and the frequency at which the electron beam can be modulated determine the display resolution.

Modern VGA displays can accommodate different resolutions, and a VGA controller circuit dictates the resolution by producing timing signals to control the raster patterns. The controller must produce synchronizing pulses at 3.3V (or 5V) to set the frequency at which current flows through the deflection coils, and it must ensure that video data is applied to the electron guns at the correct time. Raster video displays define a number of "rows" that corresponds to the number of horizontal passes the cathode makes over the display area, and a number of "columns" that corresponds to an area on each row that is assigned to one "picture element" or pixel. Typical displays use from 240 to 1200 rows and from 320 to 1600 columns. The overall size of a display and the number of rows and columns determines the size of each pixel.

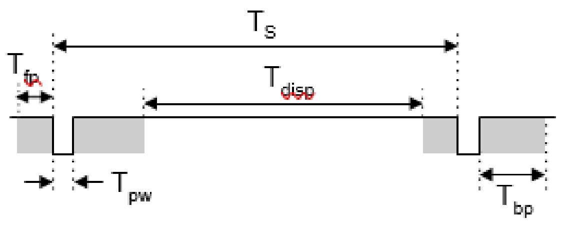


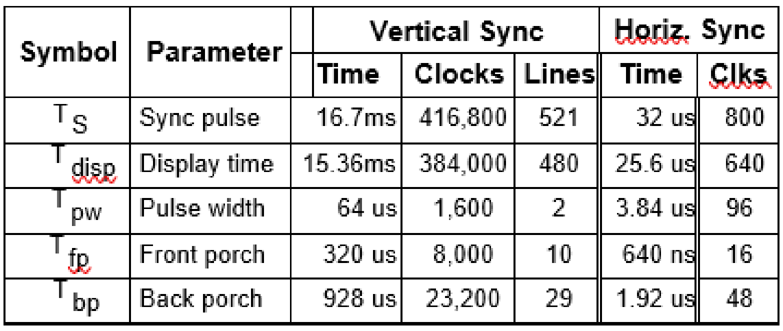
pixel 0,0
pixel 0,639
640 pixels per row are displayed during forward beam trace
Display Surface
pixel 479,0
pixel 479,639
Retrace - no information displayed during this time
Stable current ramp - information is displayed during this time
Current waveform through horizontal defletion coil
Total horizontal time
Horizontal display time
retrace time
HS
time
"front porch"
Horizontal sync signal sets retrace frequency
"back porch"

Figure 24 VGA horizontal synchronization.

Video data typically comes from a video refresh memory; with one or more bytes assigned to each pixel location (the Basys 3 uses 12-bits per pixel). The controller must index into video memory as the beams move across the display, and retrieve and apply video data to the display at precisely the time the electron beam is moving across a given pixel.

A VGA controller circuit must generate the HS and VS timings signals and coordinate the delivery of video data based on the pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the "refresh" frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical refresh frequencies falling in the 50Hz to 120Hz range. The number of lines to be displayed at a given refresh frequency defines the horizontal "retrace" frequency. For a 640-pixel by 480-row display using a 25 MHz pixel clock and 60 +/-1Hz refresh, the signal timings shown in Fig. 14 can be derived. Timings for sync pulse width and front and back porch intervals (porch intervals are the pre- and post-sync pulse times during which information cannot be displayed) are based on observations taken from actual VGA displays.





Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Figure 25 Signal timings for a 640-pixel by 480 row display using a 25 MHz pixel clock and 60 Hz vertical refresh.

A VGA controller circuit, such as the one diagramed in Fig. 15, decodes the output of a horizontal-sync counter driven by the pixel clock to generate HS signal timings. You can use this counter to locate any pixel location on a given row. Likewise, the output of a vertical-sync counter that increments with each HS pulse can be used to generate VS signal timings, and you can use this counter to locate any given row. These two continually running counters can be used to form an address into video RAM. No time relationship between the onset of the HS pulse and the onset of the VS pulse is specified, so you can arrange the counters to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation.

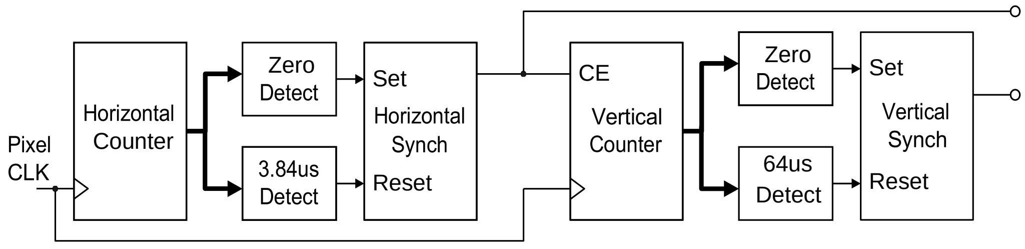


Figure 26 VGA display controller block diagram.

4.2.9 BASIC I/O

The Basys 3 board includes sixteen slide switches, five push buttons, sixteen individual LEDs, and a four-digit seven-segment display, as shown in Fig. 16. The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The five pushbuttons, arranged in a plus-sign configuration, are "momentary" switches that normally generate a low output when they are at rest, and a high output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.

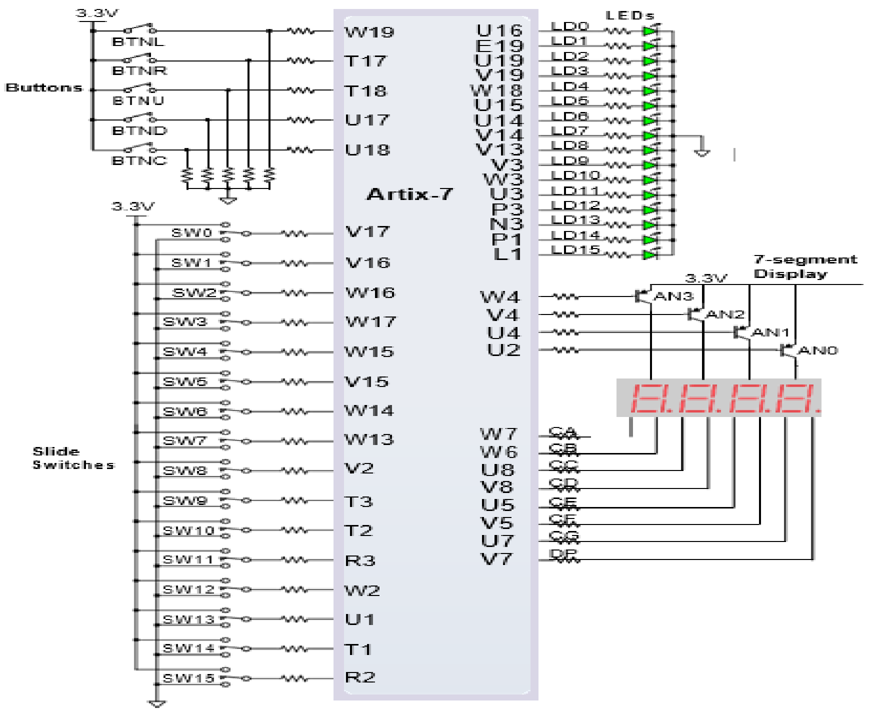


Figure 27 General purpose I/O devices on the Basys 3.

The sixteen individual high-efficiency LEDs are anode-connected to the FPGA via 330 ohm resistors, so they will turn on when a logic high voltage is applied to their respective I/O pin. Additional LEDs, which are not user- accessible, indicate power-on, FPGA programming status, and USB port status.

4.2.9.1 Seven-Segment Display

The Basys 3 board contains one four-digit common anode seven-segment LED display. Each of the four digits is composed of seven segments arranged in a "figure 8" pattern, with an LED embedded in each segment. Segment LEDs can be individually illuminated, so any one of 128 patterns can be displayed on a digit by illuminating certain LED segments and leaving the others dark, as shown in Fig. 17. Of these 128 possible patterns, the ten corresponding to the decimal digits are the most useful.

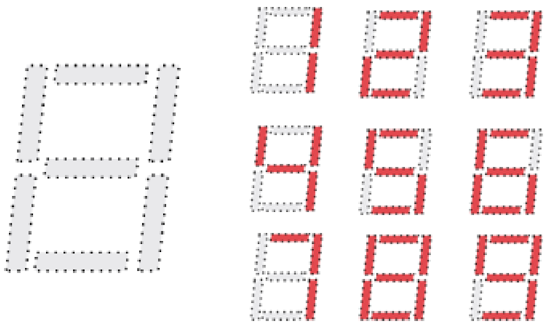


Figure 28 An un-illuminated seven-segment display and nine illumination patterns corresponding to decimal digits.

The anodes of the seven LEDs forming each digit are tied together into one "common anode" circuit node, but the LED cathodes remain separate, as shown in Fig. 18. The common anode signals are available as four "digit enable" input signals to the 4-digit display. The cathodes of similar segments on all four displays are connected into seven circuit nodes labeled CA through CG (for example, the four "D" cathodes from the four digits are grouped together into a single circuit node called "CD"). These seven cathode signals are available as inputs to the 4-digit display.

This signal connection scheme creates a multiplexed display, where the cathode signals are common to all digits but they can only illuminate the segments of the digit whose corresponding anode signal is asserted.

To illuminate a segment, the anode should be driven high while the cathode is driven low. However, since the Basys 3 uses transistors to drive enough current into the common anode point, the anode enables are inverted. Therefore, both the AN0..3 and the CA..G/DP signals are driven low when active.

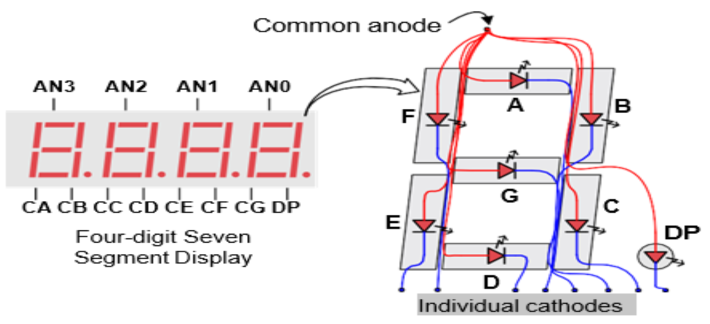


Figure 29 Common anode circuit node.

A scanning display controller circuit can be used to show a four-digit number on this display. This circuit drives the anode signals and corresponding cathode patterns of each digit in a repeating, continuous succession at an update rate that is faster than the human eye can detect. Each digit is illuminated just one-fourth of the time, but because the eye cannot perceive the darkening of a digit before it is illuminated again, the digit appears continuously illuminated. If the update, or "refresh", rate is slowed to around 45Hz, a flicker can be noticed in the display.

For each of the four digits to appear bright and continuously illuminated, all four digits should be driven once every 1 to 16ms, for a refresh frequency of about 1 KHz to 60Hz. For example, in a 62.5Hz refresh scheme, the entire display would be refreshed once every 16ms, and each digit would be illuminated for 1/4 of the refresh cycle, or 4ms. The controller must drive the cathodes

low with the correct pattern when the corresponding anode signal is driven high. To illustrate the process, if AN0 is asserted while CB and CC are asserted, then a "1" will be displayed in digit position 1. Then, if AN1 is asserted while CA, CB, and CC are asserted, a "7" will be displayed in digit position 2. If AN0, CB, and CC are driven for 4ms, and then AN1, CA, CB, and CC are driven for 4ms in an endless succession, the display will show "71" in the first two digits. An example timing diagram for a four-digit controller is shown in Fig. 19.

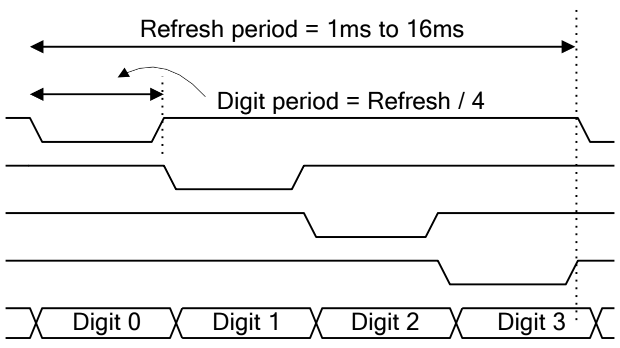


Figure 30 Four-digit scanning display controller timing diagram.

4.2.10 PMOD PORTS

The Pmod ports are arranged in a 2x6 right-angle, and are 100-mil female connectors that mate with standard 2x6pin headers. Each 12-pin Pmod port provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and11), and eight logic signals, as shown in Fig. 20. The VCC and Ground pins can deliver up to 1A of current. Pmod data signals are not matched pairs, and they are routed using best-available tracks without impedance control or delay matching. Pin assignments for the Pmod I/O connected to the FPGA are shown in Table 6.

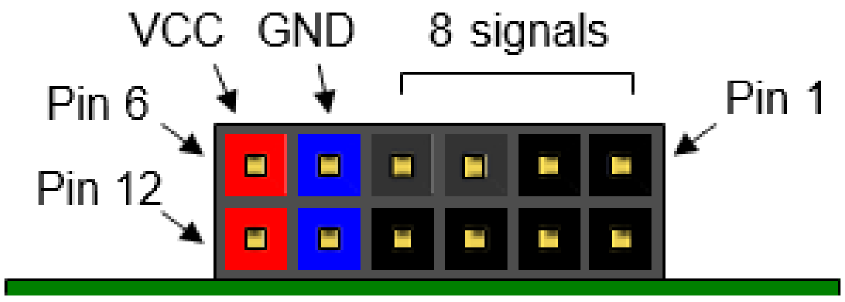
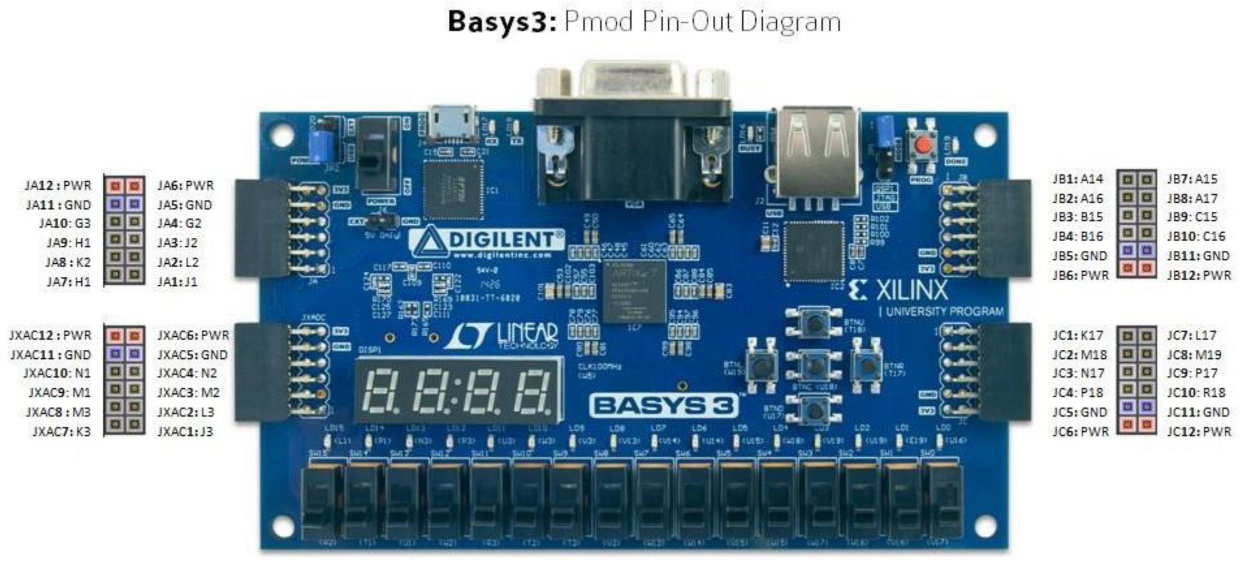


Figure 31 Pmod ports; front view as loaded on PCB.

Table 10 Basys 3 Pmod pin assignment

Pmod JA	Pmod JB	Pmod JC	Pmod XDAC
JA1: J1	JB1: A14	JC1: K17	JXADC1: J3
JA2: L2	JB2: A16	JC2: M18	JXADC2: L3
JA3: J2	JB3: B15	JC3: N17	JXADC3: M2
JA4: G2	JB4: B16	JC4: P18	JXADC4: N2
JA7: H1	JB7: A15	JC7: L17	JXADC7: K3
JA8: K2	JB8: A17	JC8: M19	JXADC8: M3
JA9: H2	JB9: C15	JC9: P17	JXADC9: M1
JA10: G3	JB10: C16	JC10: R18	JXADC10: N1

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod expansion ports to addready-made functions like A/Ds, D/As, motor drivers, sensors, and other functions. See www.digilentinc.com for more information.



4.2.10.1 DUAL ANALOG/DIGITAL PMOD

The on-board Pmod expansion port, labeled "JXADC", is wired to the auxiliary analog input pins of the FPGA. Depending on the configuration, this connector can be used to input differential analog signals to the analog-to-digital converter inside the Artix-7 (XADC). Any or all pairs in the connector can be configured either as analog input or digital input-output.

The Dual Analog/Digital Pmod on the Basys 3 differs from the rest in the routing of its traces. The eight data signals are grouped into four pairs, with the pairs routed closely coupled for better analog noise immunity. Furthermore, each pair has a partially loaded anti-alias filter laid out on the PCB. The filter does not have capacitors C33-C36. In designs where such filters are desired, the capacitors can be manually loaded by the user.

NOTE: The coupled routing and the anti-alias filters might limit the data speeds when used for digital signals. The XADC core within the Artix-7 is a dual channel 12-bit analog-to-digital converter capable of operating at 1

MSPS. Either channel can be driven by any of the auxiliary analog input pairs connected to the JXADC header. The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). The DRP also provides access to voltage monitors that are present on each of the FPGA's power rails, and a temperature sensor that is internal to the FPGA. For more information on using the XADC core, refer to the Xilinx document titled "7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter."

4.2.11 BUILT IN SELF TEST

A demonstration configuration is loaded into the SPI Flash device on the Basys 3 board during manufacturing. The source code and prebuilt bitstream for this design are available for download from the Digilent website. If the demo configuration is present in the SPI Flash device and the Basys 3 board is powered on in SPI mode, the demo project will allow basic hardware verification. Here is an overview of how this demo drives the different onboard components:

- The user LEDs are illuminated when the corresponding user switch is placed in the on position.
- The VGA port displays feedback from a USB Mouse.
- Connecting a mouse to the USB-HID Mouse port will allow the pointer on the VGA display to be controlled.
- On power-up, each digit of the seven-segment display will display a counter output from 0-9 that increments once a second.
- Pressing BTNU, BTNL, BTNR, or BTND will cause a digit of the seven-segment display to go blank.
- Pressing BTNC will reset the design.
- On power-up, a welcome message is sent over the UART. Also, every time a button is pressed a message is sent. The UART can be connected to using a terminal program with 9600 Baud, 8 data bits, 1 stop bit, and no parity.

All Basys 3 boards are 100% tested during the manufacturing process. If any device on the Basys 3 board fails test or is not responding properly, it is likely that damage occurred during transport or during use. Typical damage includes stressed solder joints and contaminants in switches and buttons resulting in intermittent failures. Stressed solder joints can be repaired by reheating and reflowing solder and contaminants can be cleaned with off-the-shelf electronics cleaning products. If a board fails test within the warranty period, it will be replaced at no cost. Contact Digilent for more details.

4.3 DEVELEPMENT FLOW

The simplified development flow of an FPGA-based system is shown below. The left portion of the flow is the refinement and programming process, in which a system is transformed from an abstract textual HDL description to a device cell- level configuration and then downloaded to the FPGA device. The right portion is the validation process, which checks whether the system meets the functional specification and performance goals. The major steps in the flow are:

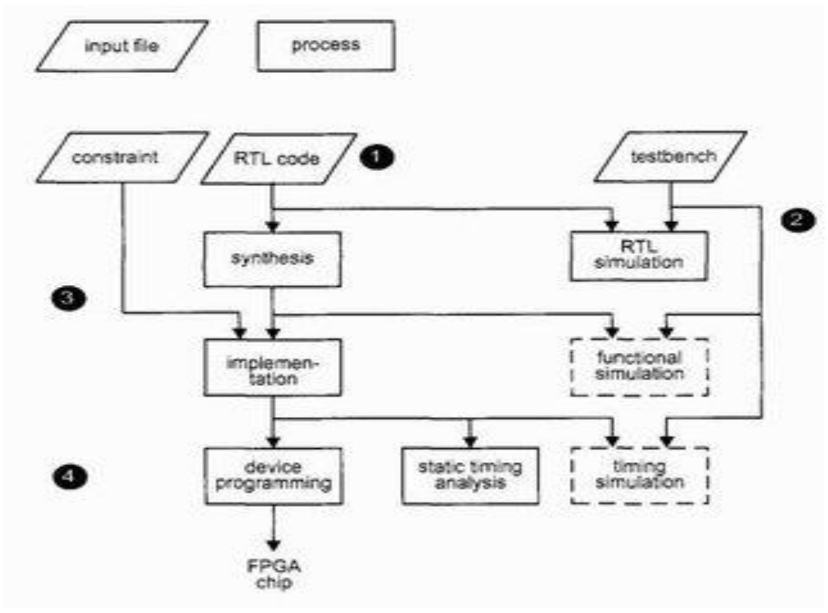


Fig 32 Development flow

a) Design Entry: Design the system and derive the HDL file(s). We may need to add a separate constraint file to specify certain implementation constraints.

b) RTL Simulation: Develop the test bench in HDL and perform RTL (Register Transfer Level) simulation. The RTL term reflects the fact that the HDL code is done at the register transfer level.

c)Synthesis: The synthesis process is generally known as logic synthesis, in which the software transforms the HDL constructs to generic level components, such as simple logic gates and FFs.

d)Implementation: The implementation process consists of three smaller processes: translate map, and place and route. The translate process merges multiple design files to a single netlist. The map process, which is generally known as technology mapping, maps the generic gates in the netlist to FPGA logic cells and IOBs. The place and route process, which is generally known as placement and routing, derives the physical layout inside the FPGA chip. It places the cells in physical locations and determines routes to connect various signals. In the Xilinx flow, static timing analysis, which determines various timing parameters, such as maximal propagation delay and maximal clock frequency, is performed at the end of the implementation process.

e) Generate and download the programming file: In this process, a configuration file is generated according to the final netlist. This file is downloaded to an FPGA device serially to configure the logic cells and switches. The physical circuit can be verified accordingly.

The optional functional simulation can be performed after synthesis, and the optional timing simulation can be performed after implementation. Functional simulation uses a synthesized netlist to replace the RTL description and checks the correctness of the synthesis process. Timing simulation uses the final netlist, along with detailed timing data, to perform simulation. Because of the complexity of the netlist, functional and timing simulation may require a significant amount of time. If we follow good design and coding practices, the HDL code will be synthesized and implemented correctly. We only need to use RTL simulation to check the correctness of the HDL code and use static timing analysis to examine the relevant timing information. Both functional and timing simulations can be omitted from the development flow.

4.4 Overview of VERILOG

Verilog, standardized as IEEE 1364, is a hardware description language (HDL) used to model electronics systems. It is most commonly used in the design and verification of digital circuits at the regular – transfer level of abstraction. It is also used in the verification of analog circuits and mixed signal circuits HDLs allows the design to be simulated earlier in the design cycle in order to correct errors or experiment with different architectures. Designs described in HDL are technology independent, easy to design and debug, and are usually more readable than schematics, particularly for large circuits.

Verilog can be used to describe designs at four levels of abstraction:

Algorithmic level (much like a code if, case and loop statements).

- Register transfer level (RTL uses registers connected by Boolean equations
- Gate level (interconnected AND, NOR etc.).
- Switch level (the switches are MOS transistors inside gates).

A Verilog design consists of a hierarchy of modules. Modules encapsulate design hierarchy, and communicate with other modules through a set of declared input, output and bidirectional ports. Internally, a module can contain any combination of the following: net/variable declarations (wire, reg, integer etc.), concurrent and sequential statement blocks and instances of other modules (sub – hierarchies).

4.4.1 Features of Verilog HDL

Verilog HDL offers many useful features for hardware design

- Verilog (verify logic) HDL is a general-purpose hardware description language that is easy to learn and use. It is similar in syntax to the C programming language. Designers with C programming experience will find it easy to learn Verilog HDL.
- Verilog HDL allows different levels of abstraction to be mixed in the same model. Thus, a designer can define a hardware model in terms of switches, gates, RTL or behavioral code. Also, a designer needs to learn only one language for stimulus and hierarchical design.
- Most popular logic synthesis tools support Verilog HDL. This makes it the language of choice for designers.
- All fabrication vendors provide Verilog HDL libraries for post logic synthesis simulation. Thus, designing a chip in Verilog HDL allows the widest choice of vendors.
- The programming language interface (PLI) is a powerful feature that allows the user to custom C code to interact with the internal data structures of Verilog. Designers can customize a Verilog HDL simulator to their need with the Programming language interface (PLI).

4.4.2 Module Declaration

A module is the principal design entity in Verilog. The first line of a module declaration specifies the name and port list (arguments). The next few lines specifies the I/O type (input, output or in out) and width of each port. The default port width is 1 bit. Then the port variables must be declared wire, reg. The default is wire. Typically, inputs are wire since their data is latched outside the module. Outputs are type reg if their signals were stored inside an always or initial block.

Syntax

```
Module model name (port list)
Input[msb:lsb] input_port_list;
Output[msb:lsb] output_port_list;
inout[msb:lsb] inout_port_list;
…………Statements…………….
endmodule
```

Example

```
module add sub (add, in1, in2, out);
input add;
input [7:0]in, in2;
wire in1, in2;
output [7:0]out;
reg out;
…………..Statements…………
endmodule
```

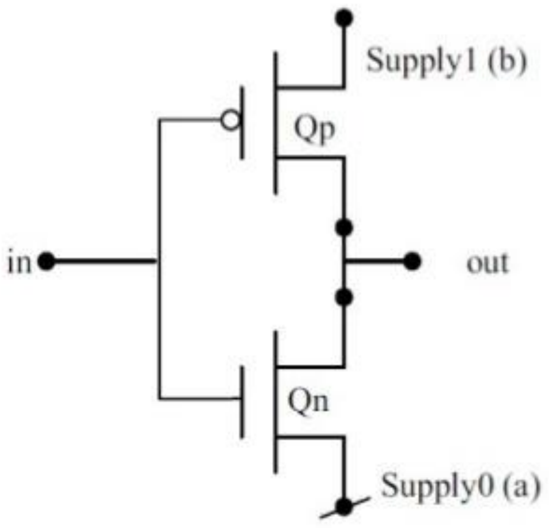
Verilog has four levels of modeling:

1) The Switch level modeling.
2) Gate level modeling.
3) The Data flow level.
4) The Behavioral level.

1)Switch level modeling

Switch level modeling forms the basic level of modeling digital circuits. The switches are available as a primitives in Verilog; they are central to design description at this level. Basic gates can be defined in terms of such switches. Switch-level modeling is a recently developed design and analysis methodology for MOS VLSI circuits. At the switch level, important features of MOS circuits can be directly modeled using a moderate number of discrete parameters, including switch states, resistance, capacitance, and bidirectional signals. Switch-level models, provide more accurate behavioral and structural information than gate-level logical models, while avoiding the high computational cost associated with analog electrical models. It provides a level of abstraction between the logic and analog-transistor levels of abstraction, describing the interconnection of transmission gates which are abstractions of individual mos and cmos transistors. The design of MOS technology electronic circuits requires functional level simulations, as well as switch and circuit-level simulations. Functional simulations are necessary to understand the behavior independently of the implementation details.

CMOS inverter:



```
module inv (in, out );
output out;
input in;
supply0 a;
supply1 b;
nmos (out, a, in );
pmos (out, b, in);
endmodule
```

Fig 33 CMOS inverter

2) Gate Level Modeling

Modelling done at this level is usually called gate level modelling as it involves gates and has a one to one relation between a hardware schematic and the Verilog code. Verilog supports a few basic logic gates known as primitives as they can be instantiated like modules since they are already predefined. In general, *gate-level modelling* is used for implementing lowest *level* modules in a design like, full-adder, multiplexers, etc. *Verilog* HDL has *gate* primitives for all basic *gates*. *Gate* primitives are predefined in *Verilog*, which are ready to use. Multiple input *gate* primitives include and, nand, or, nor, xor and xnor. Designer should know the gate level diagram of the design.

Example

```
module or_gate (out, a, b, c, d);
input a, b, c, d;
wire x, y;
output out;
or or1(x, a, b);
or or2(y, c, d);
or orfinal(out, x, y);
endmodule
```

3)Data flow level modelling

Dataflow modelling provides the means of describing combinational circuits by their function rather than by their gate structure. Dataflow modelling uses a number of operators that act on operands to produce the desired results. Verilog HDL provides about 30 operator types.

Dataflow modelling uses continuous assignments and the keyword assign. A continuous assignment is a statement that assigns a value to a net. The datatype net is used in Verilog HDL to represent a physical connection between circuit elements. The value assigned to the net is specified by an expression that uses operands and operators. As an example, assuming that the variables were declared, a2-to-1 multiplexer with data inputs A and B, select input S, and output Y is described with continuous assignment.

```
 assign Y= (A & S) | (B & S)
```

Example

The dataflow description of a 2-to-4-line decoder is shown in HDL below. The circuit is defined with four continuous assignment statements using Boolean expressions, one for each output. // Dataflow description of 2-to-4 line decoder with enable input (E) module decoder_df (A,B,E,D);

```
 input A,B,E;
 output [3,:0] D;
 assign D[3] =~(~A & ~B & ~E);
 assign D[2] =~(~A & B & ~E);
 assign D[1] =~( A & ~B & ~E);
 assign D[0] =~( A & B & ~E);
endmodule
```

4)Behavioural level modelling

This is the highest level of abstraction provided by Verilog HDL. A module can be implemented in terms of the desired design algorithm without concern for the hardware implementation details. It specifies the circuit in terms of its expected behaviour. It specifies the circuit in terms of its expected behaviour. It is the closest to a natural language description of the circuit functionality, but also the most difficult to synthesize.

All that a designer need is the algorithm of the design, which is the basic information for any design. This level simulates the behavioural level of the circuits and development rate in this level is highest. Although the development rate in this abstraction level is high there are some drawbacks such as the delay modelling is not possible. In practice any circuit is first implemented in this level to understand the theoretical possibility of the circuit and then it is implemented in at a lower level to analyse the practical aspects. This level of Verilog has blocking and non-blocking assignment. Blocking assignment is sequential nature and using the combination of both assignments, complex sequential can be modelled with ease.

The abstraction in this modelling is as simple as writing the logic in C language. This is a very powerful abstraction technique. All that a designer needs are the algorithm of the design, which is the basic information for any design. This level is very important because with the increasing complexity of digital design, it has become vitally important to make wise design decisions early in a project. Designers need to be able to evaluate the trade-offs of various architectures and algorithms before they decide on the optimum architecture and algorithm to implement in hardware. Only after the high-level architecture and algorithm are finalized, designers start focusing on building the digital circuit to implement the algorithm. Most of the behavioural modelling is done using two important constructs: initial and always. All the other behavioural statements appear only inside these two structured procedure constructs.

Initial construct

The statements which come under the initial construct constitute the initial block. The initial block is executed only once in the simulation, at time 0. If there are more than one initial blocks, than all the initial blocks are executed concurrently. The initial construct is used as follows:

```
Initial
Begin
Reset = 1'b0;
clk = 1'b1;
end
```

In the first initial block there is more than one statements hence they are written between begin and end. If there is only one statement then there is no need to put begin and end.

Always construct

The statements which come under the always construct constitute the always block. The always block starts at time 0, and keeps on executing all the simulation time. It works like an infinite loop. It is generally used to model a functionality that is continuously repeated.

```
always
#5 clk = ~clk;
initial
clk = 1'b0;
```

The above code generates a clock signal clk, with a time period of 10units. The initial blocks initiates the clk value to 0 at time 0. Then after every 5 units of time it is toggled, hence we get a time period of 10units. This is the general way to generate a clock signal for use in testbenches.

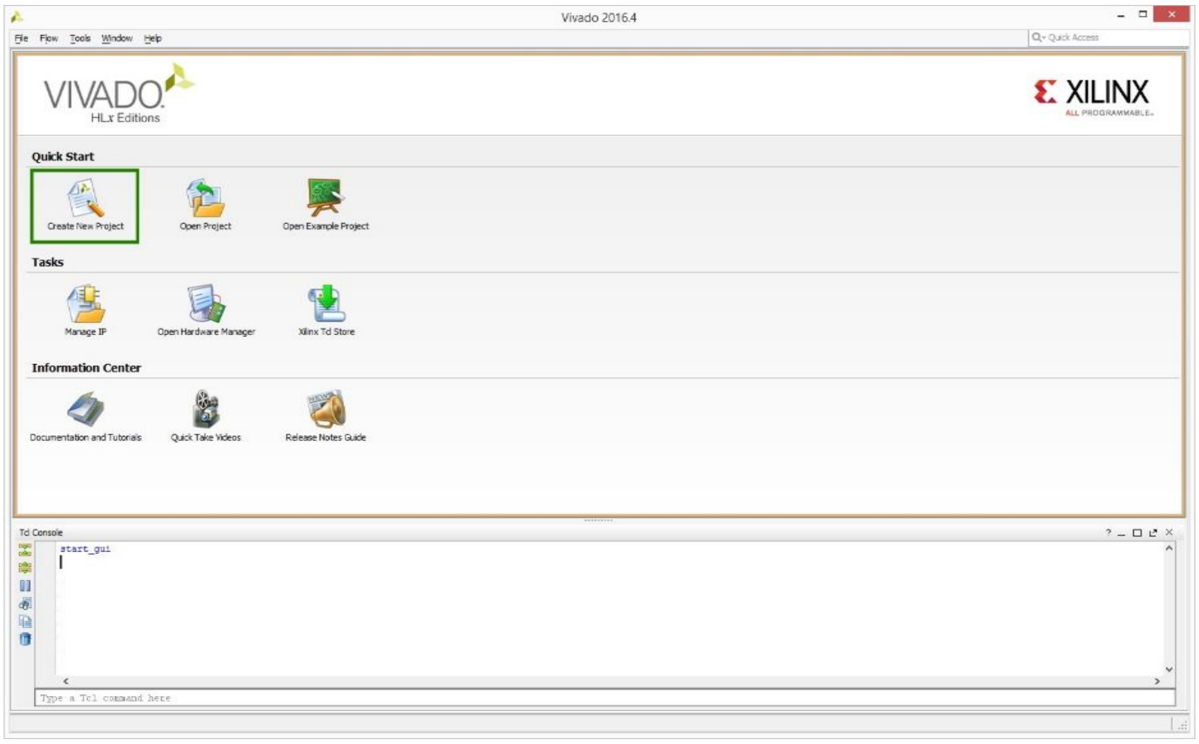
4.5 Overview of EDA (Electronic Design Automation) software

Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis.

Setting up a Vivado project involves the following steps-

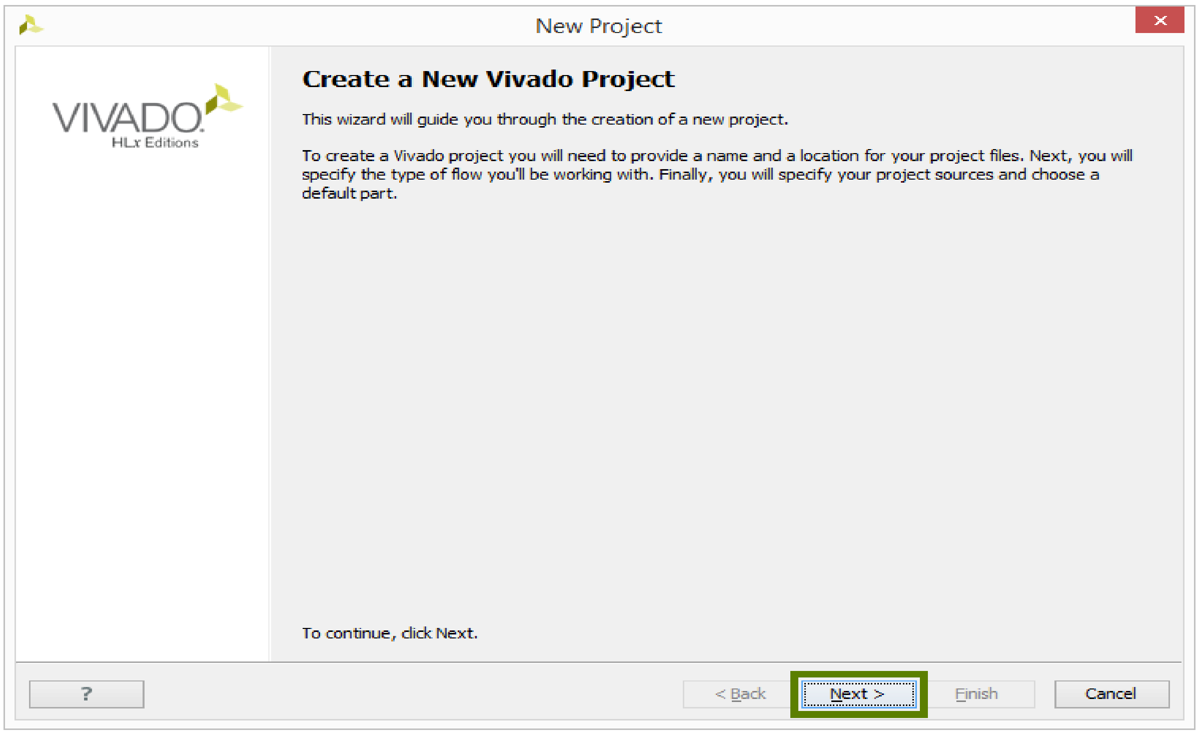
Creating a New Project

After launching Vivado, from the startup page click the "Create New Project" icon. Alternatively, you can select File ➔ New project



```
start_gui
```

The New Project wizard will launch, click the "Next>" button to proceed.



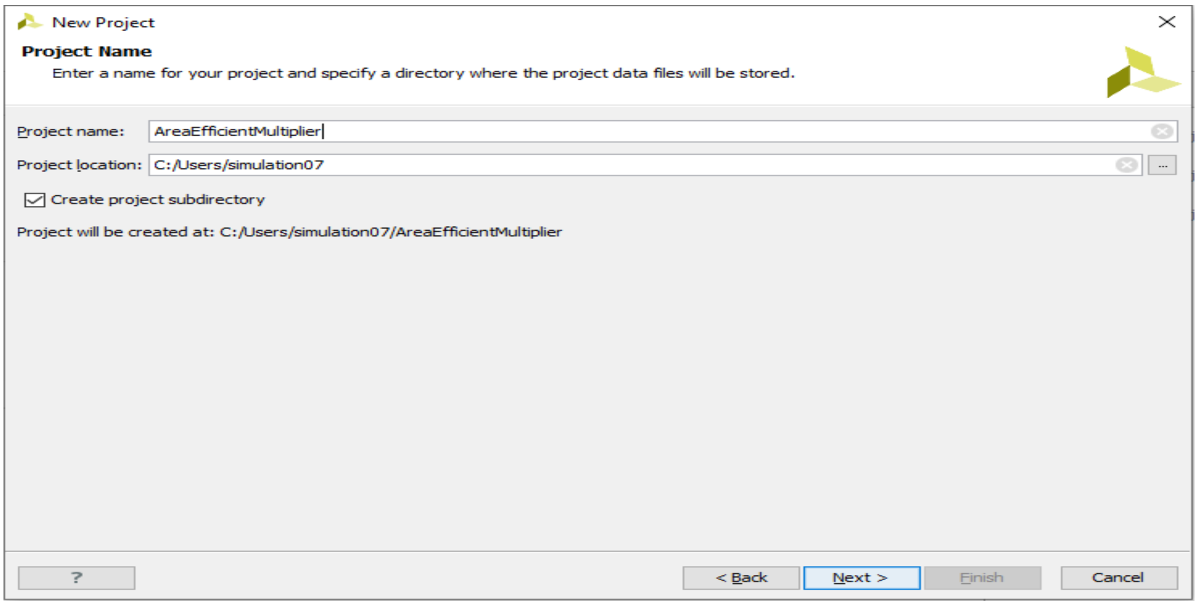
Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.

To continue, click Next.

Enter a project name and select a project location. Make certain there are NO SPACES in either! It's not a bad idea to only use letters, numbers, and underscores as well. If necessary simply create a new directory for your Xilinx Vivado projects in your root drive (e.g. C:/Vivado). You will likely always want to select the "create project sub-directory" check-box as well. This keeps the things neatly organized with a directory for each project and helps avoid problems. Click the "Next>" button to proceed.



Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

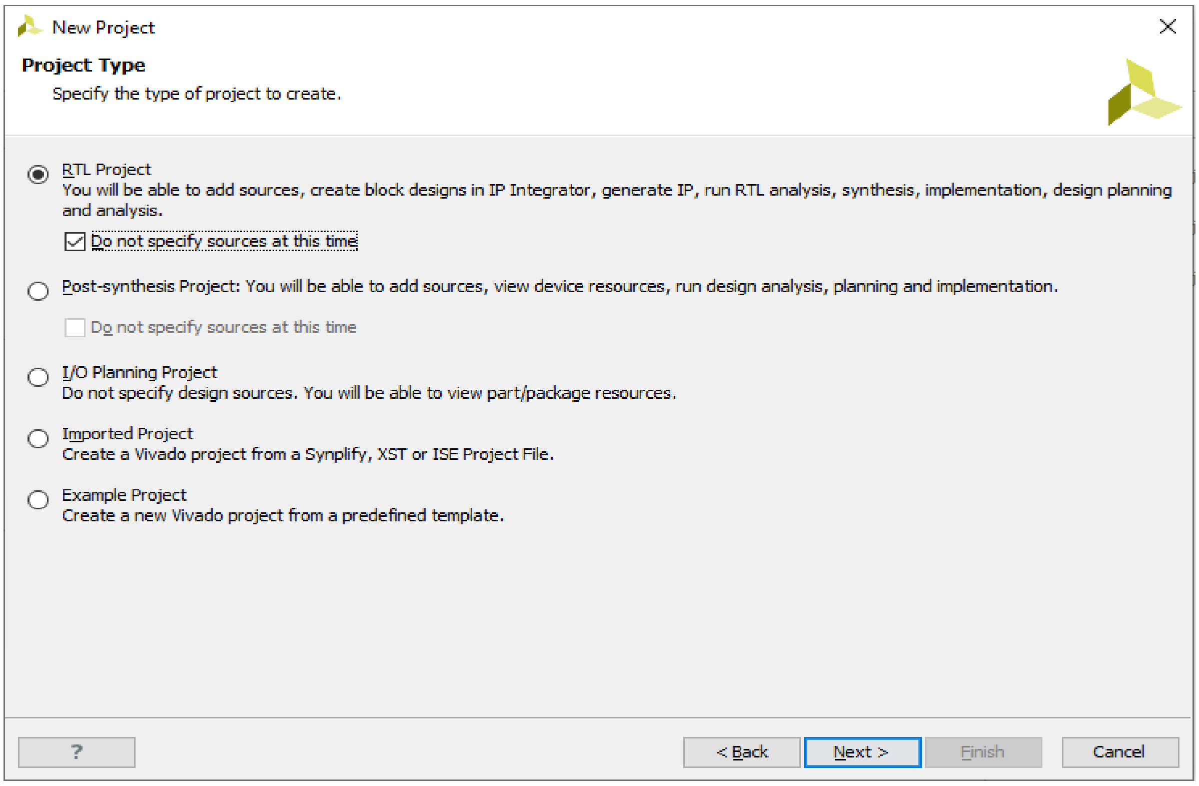
Project name: AreaEfficientMultiplier

Project location: C:/Users/simulation07

☑ Create project subdirectory

Project will be created at: C:/Users/simulation07/AreaEfficientMultiplier

Select the "RTL Project" radial and select "Do not specify sources at this time" check -box. If you don't select the check-box the wizard will take you through some additional steps to optionally add pre existing items such as VERILOG or Verilog source files, Vivado IP blocks, and. XDC constraint file for device pin amd timing configuration. For this first project you will add necessary items later. Click the "Next>" button to proceed



New Project

Project Type

Specify the type of project to create.

[✓ RTL Project]
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

[✓ Do not specify sources at this time]

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.

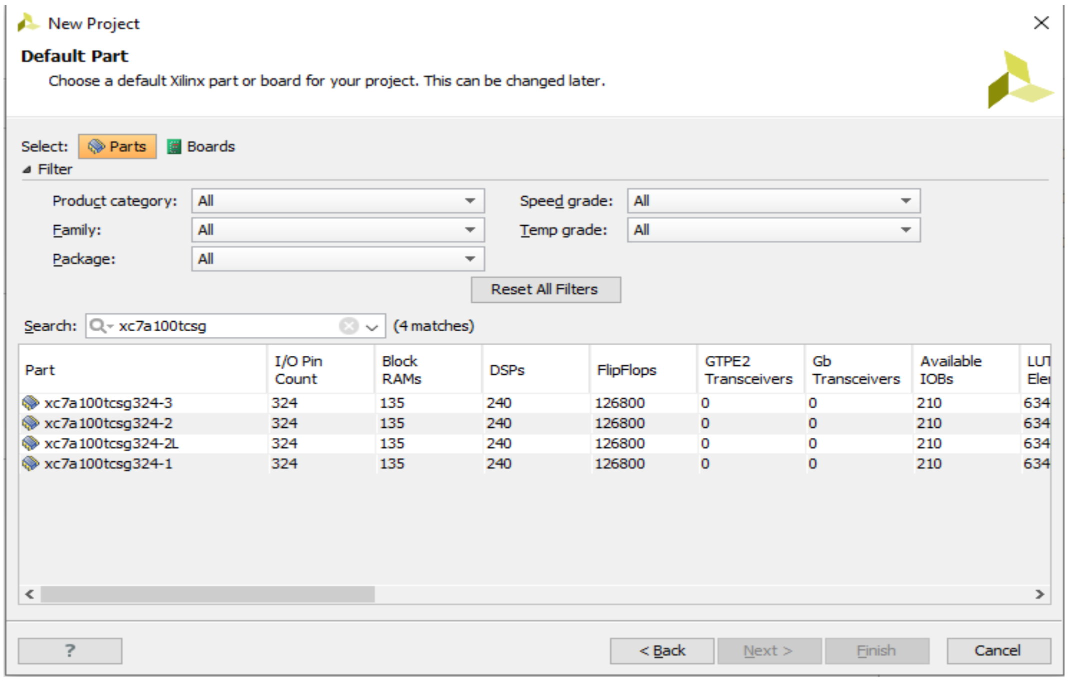
Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

Once you select the RTL project, Click on next button.



New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: [✓ Parts] Boards

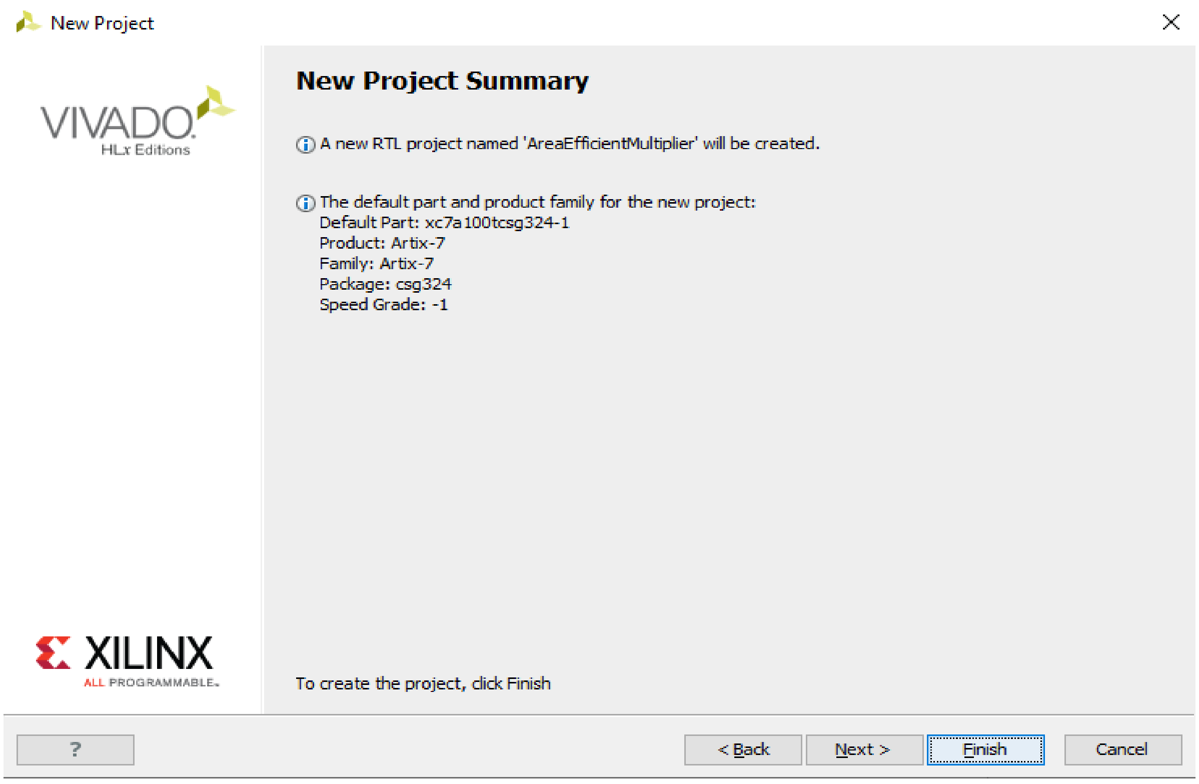
Filter

Product category: All
Family: All
Package: All
Speed grade: All
Temp grade: All

Reset All Filters

Search: xc7a100tcsg (4 matches)

Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GTPE2 Transceivers	Gb Transceivers	Available IOBs	LUT Ele
xc7a100tcsg324-3	324	135	240	126800	0	0	210	634
xc7a100tcsg324-2	324	135	240	126800	0	0	210	634
xc7a100tcsg324-2L	324	135	240	126800	0	0	210	634
xc7a100tcsg324-1	324	135	240	126800	0	0	210	634



New Project Summary

A new RTL project named 'AreaEfficientMultiplier' will be created.

The default part and product family for the new project:
Default Part: xc7a100tcsg324-1
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -1

To create the project, click Finish

Click the “Finish” button and Vivado will proceed to create your project as specified.

STEPS FOR DESIGN ENTRY/ IMPLEMENTATION:

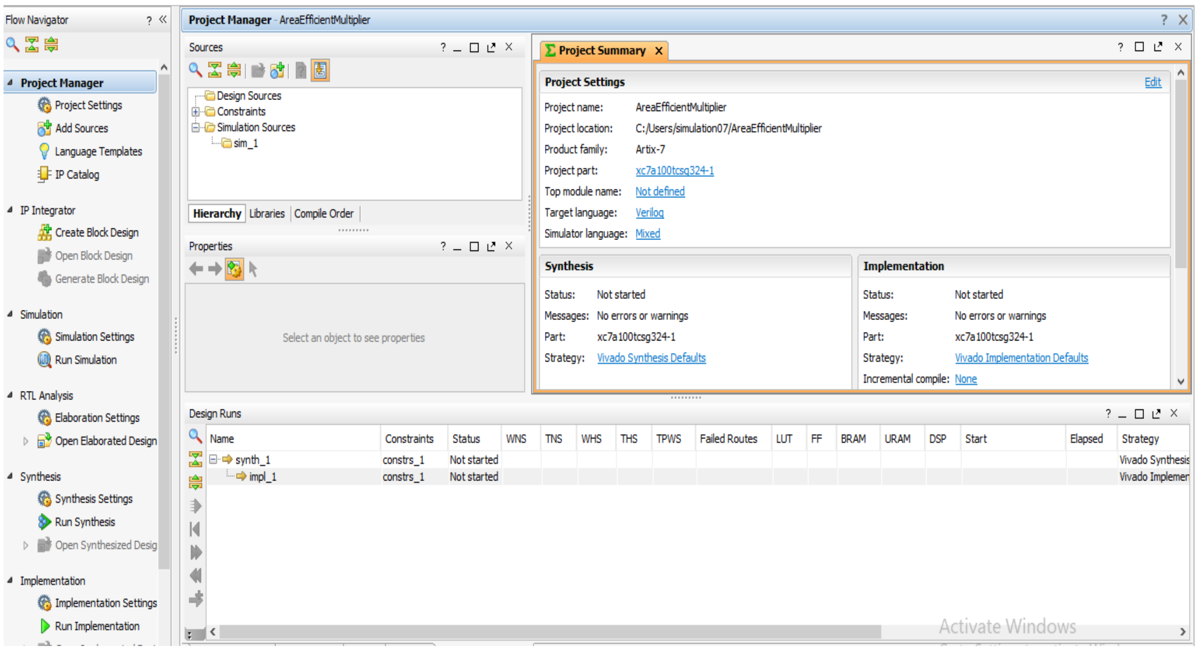
Working through the basic project flow

The Vivado project window contains a lot of information, and the information displayed can change depending on what part of the design currently have open as you work through the steps of your project. Keep this in mind as you work through this guide, because if you don’t see a specific sub window or sub window tab it’s possible you are’nt in the correct part of the design.

The “Flow Navigator” on the left side of the screen has all the major project phases organized from top to bottom in their natural chronological order. You begin in the “project manager” portion of the flow and the header at the top of the screen next to the flow navigator reflects this. This header and the corresponded highlighted section in the flow navigator will tell you which phase of the design you have opened.

Project Manager

Now click on “Add sources” under the project manager phase of the flow navigator.



Project Settings Edit

Project name:	AreaEfficientMultiplier
Project location:	C:/Users/simulation07/AreaEfficientMultiplier
Product family:	Artix-7
Project part:	xc7a100tcsg324-1
Top module name:	Not defined
Target language:	Verilog
Simulator language:	Mixed

Synthesis

Status:	Not started
Messages:	No errors or warnings
Part:	xc7a100tcsg324-1
Strategy:	Vivado Synthesis Defaults

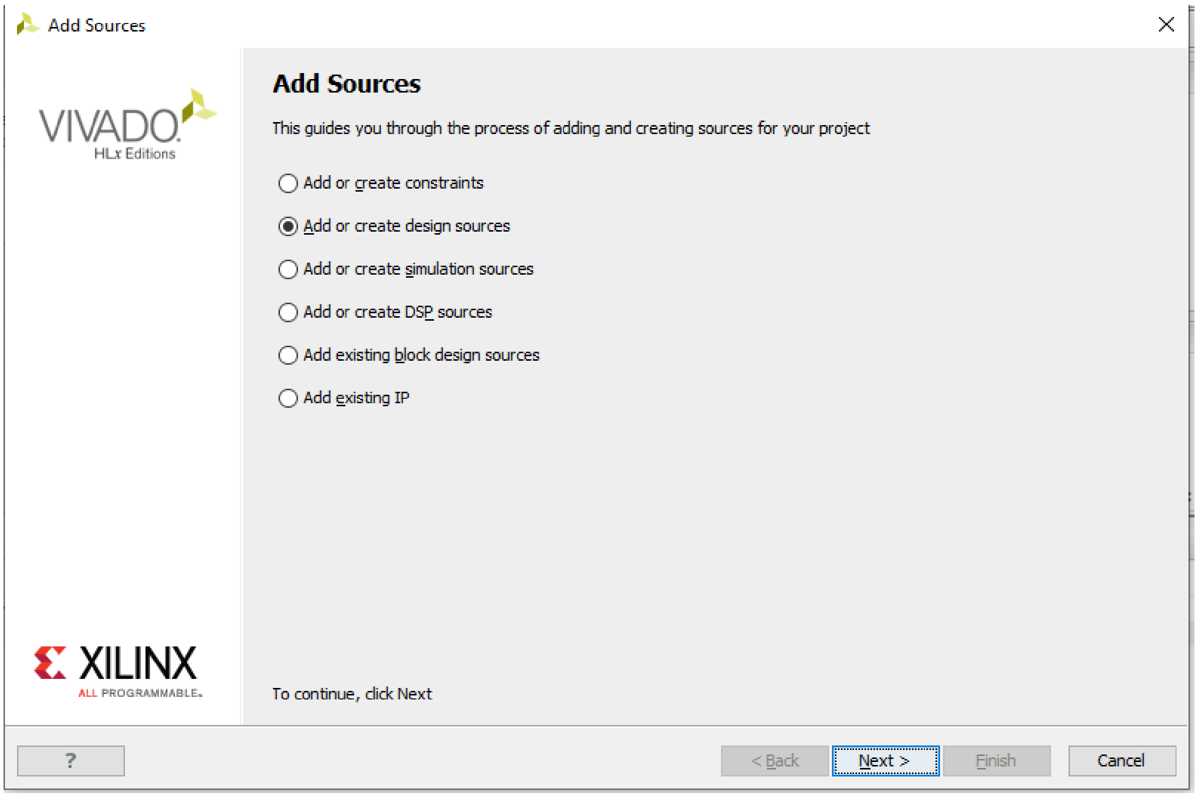
Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7a100tcsg324-1
Strategy:	Vivado Implementation Defaults
Incremental compile:	None

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Strategy
synth_1	constrs_1	Not started														Vivado Synthesis
impl_1	constrs_1	Not started														Vivado Implemen

Select the "Add or create design sources" radial and then click the "Next" button.



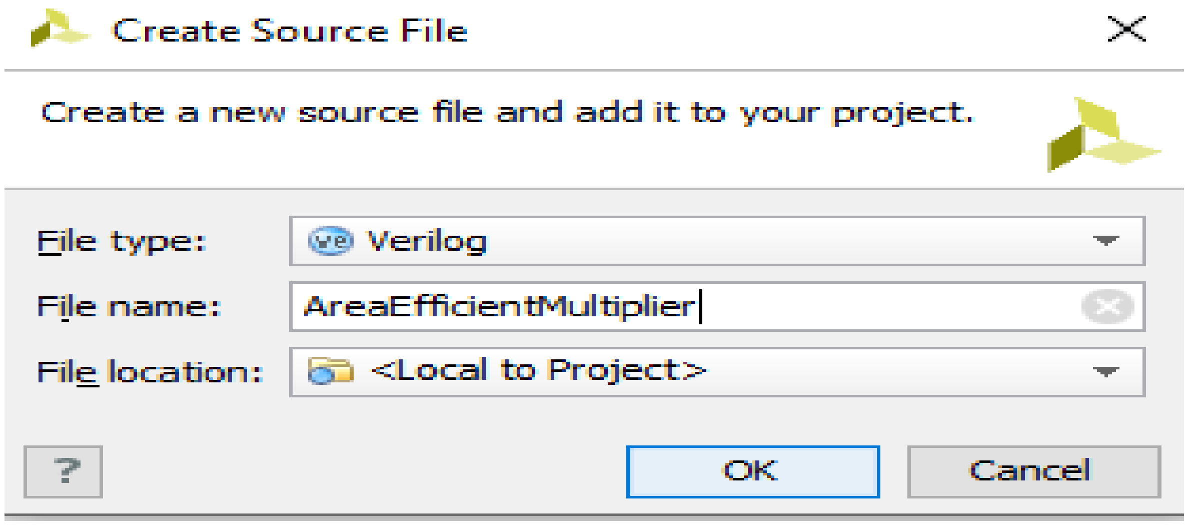
Add Sources

This guides you through the process of adding and creating sources for your project

- ○ Add or create constraints
- ● Add or create design sources
- ○ Add or create simulation sources
- ○ Add or create DSP sources
- ○ Add existing block design sources
- ○ Add existing IP

To continue, click Next

Click the "Create file" button or click the Green "+"symbol in the upper left corner and select the "create file" option.



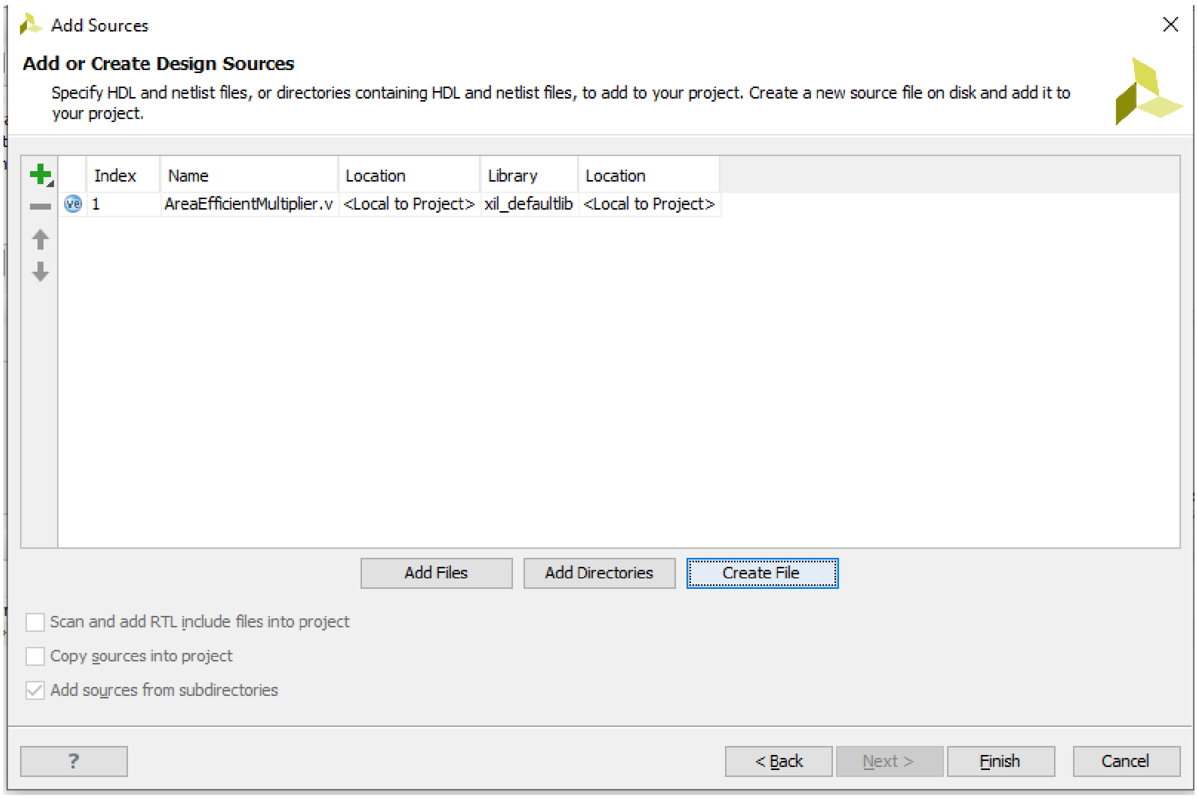
Create Source File

Create a new source file and add it to your project.

File type:	Verilog
File name:	AreaEfficientMultiplier
File location:	<Local to Project>

Make sure the options shown are selected in the "create source file" pop up, and for the sake of following enter "blinky" for the file name. Click the ok button when finished.

Click the "finish button" and Vivado will then bring up the define module name



Add Sources

Add or Create Design Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project.

Index	Name	Location	Library	Location
1	AreaEfficientMultiplier.v	<Local to Project>	xil_defaultlib	<Local to Project>

- [ ] Scan and add RTL include files into project
- [ ] Copy sources into project
- [✓] Add sources from subdirectories

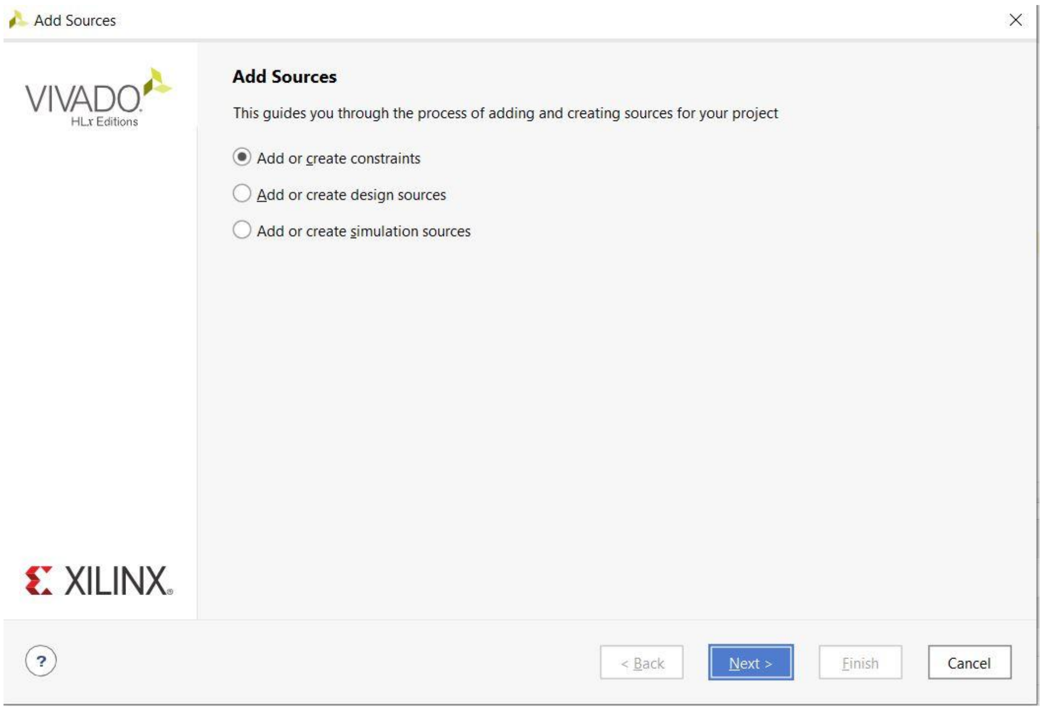
You can use the "define module" window to automatically write some of the verilog code. Additional "I/O definitions" can be added by either clicking the green "+" symbol in the upper left or by simply clicking on the next empty line.

Note that if you would rather write your own code from scratch you can just simply click the “cancel” button and Vivado will create a completely blank Verilog source file inside your project. If you click the “OK” button without defining any “I/O definitions” Vivado will still write the basic Verilog code structure but the port definition will be empty and commented and you can write down the required remaining program.

STEPS FOR CONSTRAINTS FILE CREATION

Click on “Add sources” under the project manager phase of the Flow navigator.

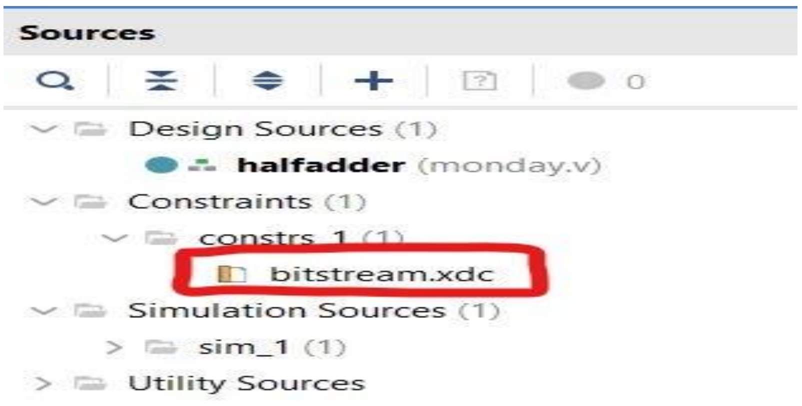
Select the “Add or create constraints” radial and then click the “Next>”button


Add Sources

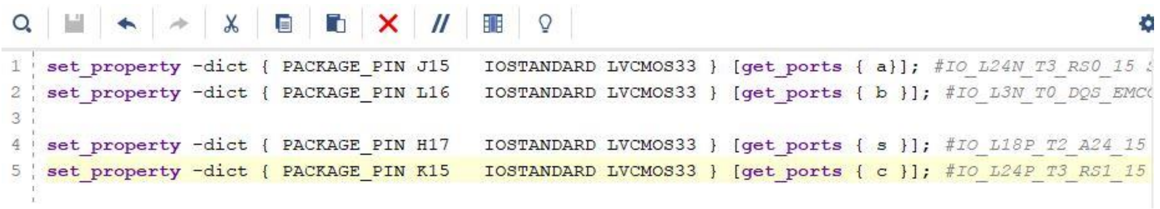
This guides you through the process of adding and creating sources for your project

(●) Add or create constraints
( ) Add or create design sources
( ) Add or create simulation sources

Then appears a popup asking for file name of the constraint file. Assign name to the constraint file and make sure **that there are no spaces!** and then click “OK”.



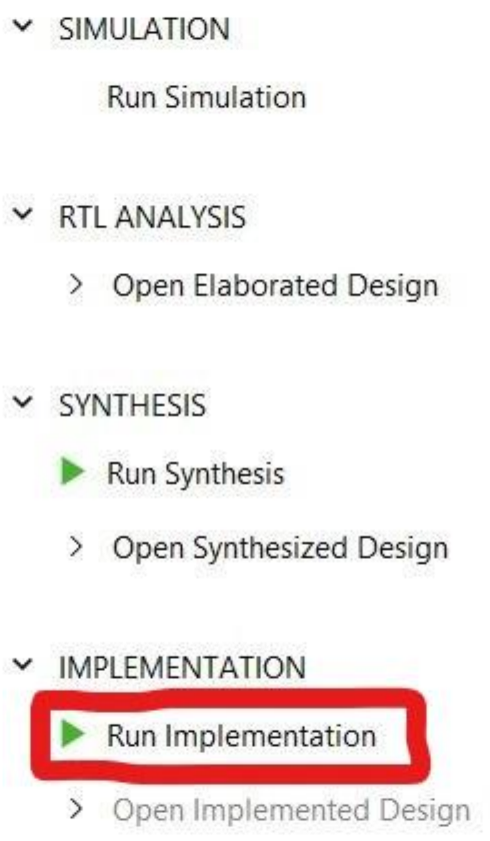
Write the bit file according to the requirement. The required memory locations are mapped to the program variables.



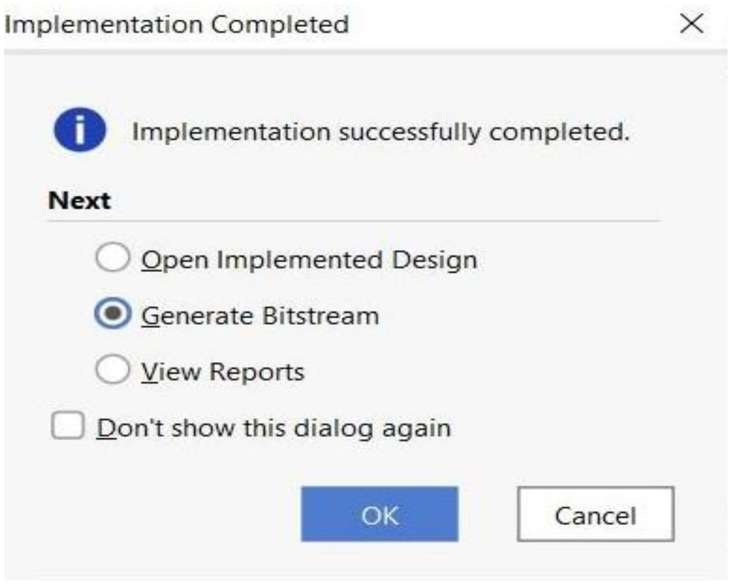
```
set_property -dict { PACKAGE_PIN J15   IOSTANDARD LVCMOS33 } [get_ports { a}]; #IO_L24N_T3_RS0_15
set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { b }]; #IO_L3N_T0_DQS_EMC

set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports { s }]; #IO_L18P_T2_A24_15
set_property -dict { PACKAGE_PIN K15   IOSTANDARD LVCMOS33 } [get_ports { c }]; #IO_L24P_T3_RS1_15
```

The above written bit file is for half adder. The input variables a and b are mapped to input switch locations and the output variables s, c are mapped to output LED locations. In this way a bit file can be written according to our program requirements. We can also access locations other than switches and LEDs like LCD display, clock, buttons and Pmod Headers. The Pmod Headers are used for external interfacing.

After writing bit file click on “Run Implementation”



After successfully completing the implementation, a pop up appears as follows


Implementation Completed

Implementation successfully completed.

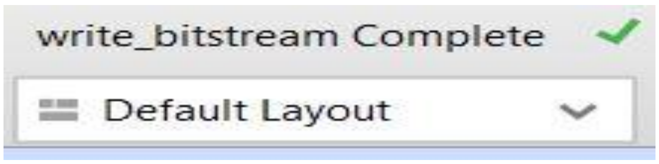
Next

Open Implemented Design [✓ Generate Bitstream] View Reports

Don't show this dialog again

OK Cancel

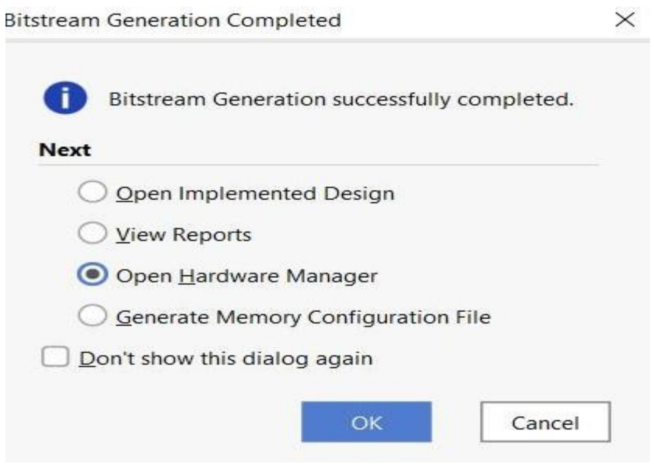
Click on “Generate Bitstream” and then “OK”.


write_bitstream Complete ✓

Default Layout

This is an indication for completion of the generation of the bitstream which appears on top right corner.

Now we have to connect to hardware device to target the device


Bitstream Generation Completed

Bitstream Generation successfully completed.

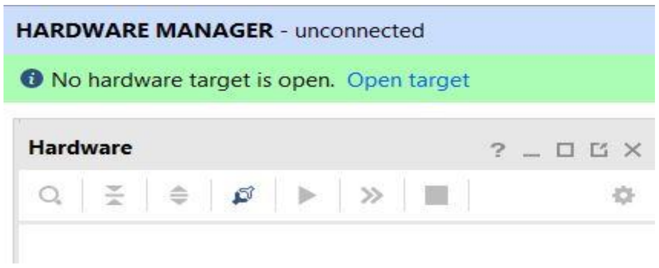
Next

Open Implemented Design View Reports [✓ Open Hardware Manager] Generate Memory Configuration File

Don't show this dialog again

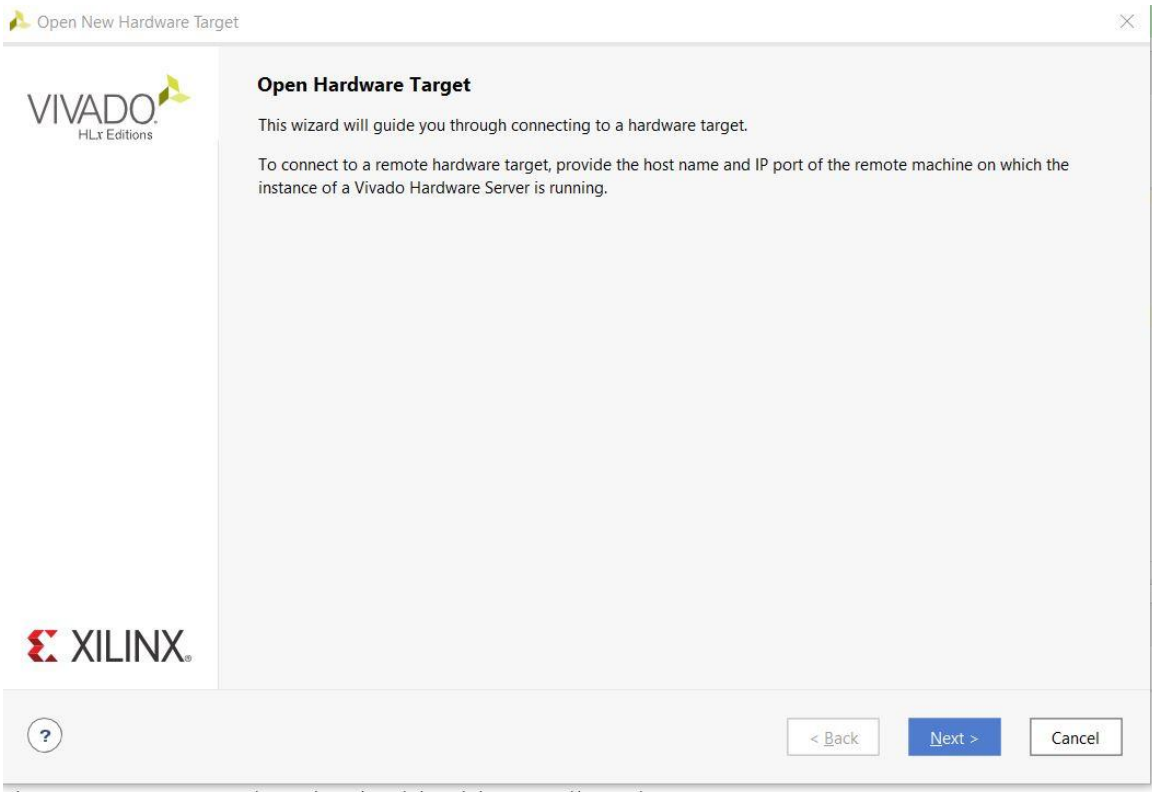
OK Cancel

Click on “Open Hardware Manager” and then “OK”


HARDWARE MANAGER - unconnected

No hardware target is open. Open target

Click on “Open Target” to target a device. The Open New Hardware Target wizard will launch, click the “Next>” button to proceed.

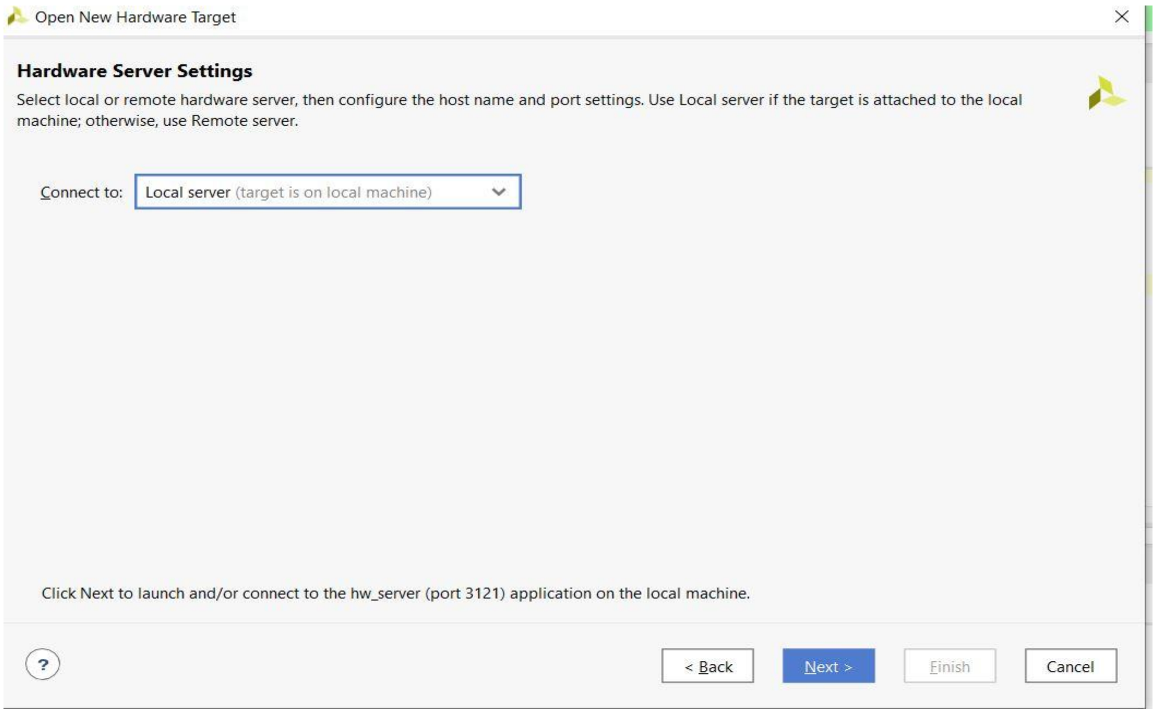

Open New Hardware Target

Open Hardware Target

This wizard will guide you through connecting to a hardware target.

To connect to a remote hardware target, provide the host name and IP port of the remote machine on which the instance of a Vivado Hardware Server is running.

Select the “local server(target is on local machine)” from the drop down if it isn’t already, and then click the “Next>”button to proceed. Vivado will work for a moment to find any valid target devices connected to your local machine.

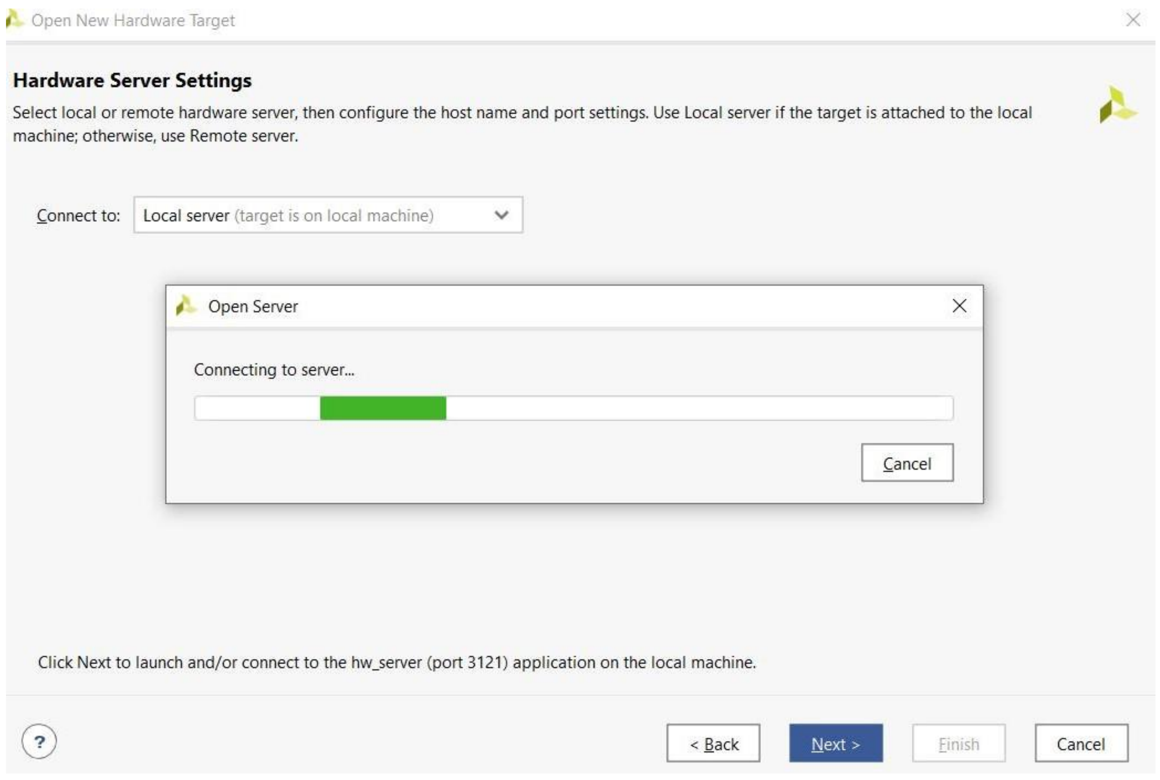

Open New Hardware Target

Hardware Server Settings

Select local or remote hardware server, then configure the host name and port settings. Use Local server if the target is attached to the local machine; otherwise, use Remote server.

Connect to: Local server (target is on local machine)

Click Next to launch and/or connect to the hw_server (port 3121) application on the local machine.


Open New Hardware Target

Hardware Server Settings

Select local or remote hardware server, then configure the host name and port settings. Use Local server if the target is attached to the local machine; otherwise, use Remote server.

Connect to: Local server (target is on local machine)

Open Server

Connecting to server...

Click Next to launch and/or connect to the hw_server (port 3121) application on the local machine.

Select your specific Hardware device. Click the "Finish" button and Vivado will attempt to connect to your specified hardware. Now click "Program device" under the program and debug phase of the Flow Navigator and then your specific device from the menu that appears. After sometime the device will be programmed and the required outputs (LED's) can be obtained by varying the inputs(switches)

CHAPTER 5
RESULTS AND CONCLUSIONS

5.1 Software: Xilinx Vivado

- We have written code for design of CSD multiplier using verilog language.
- Verilog is a Hardware Description Language which is used to design and describe digital circuits.
- The Verilog HDL is an IEEE standard - number 1364. Verilog is intended to be used for verification through simulation, for timing analysis, for test analysis and for logic synthesis.
- Verilog is an easier language as its syntax is based on C language. Verilog supports a design at many levels of abstraction. The major three are? Behavioral level, Register-transfer level and Gate level. We have simulated the code in Vivado software and analyzed the results.

5.2 Simulation Results of CSD Multiplier

a) RTL Diagram

Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. The figure below represents the RTL diagram of 8-bit CSD multiplier designed.

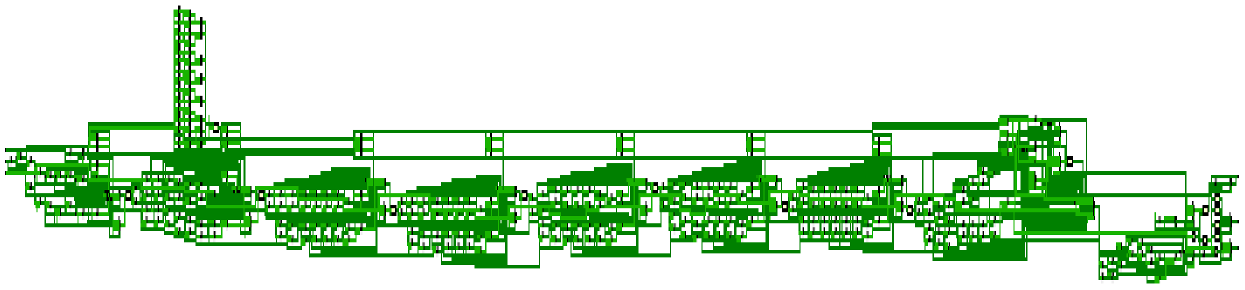


FIG 34 RTL diagram

b) Synthesized Schematic Diagram

The Synthesized Schematic diagram for the above RTL diagram is as shown. It represents how the actual components are connected on the artix-7 Fpga board.

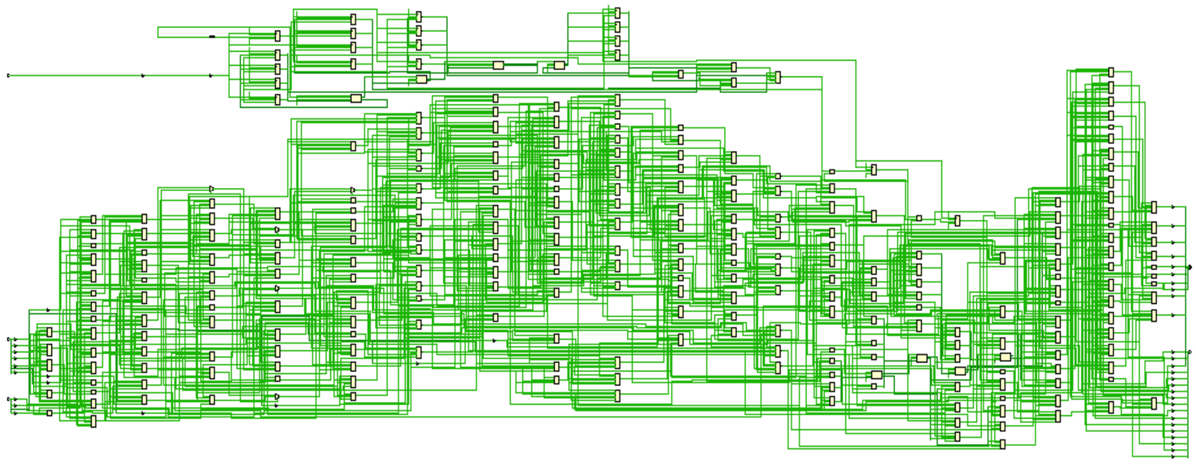
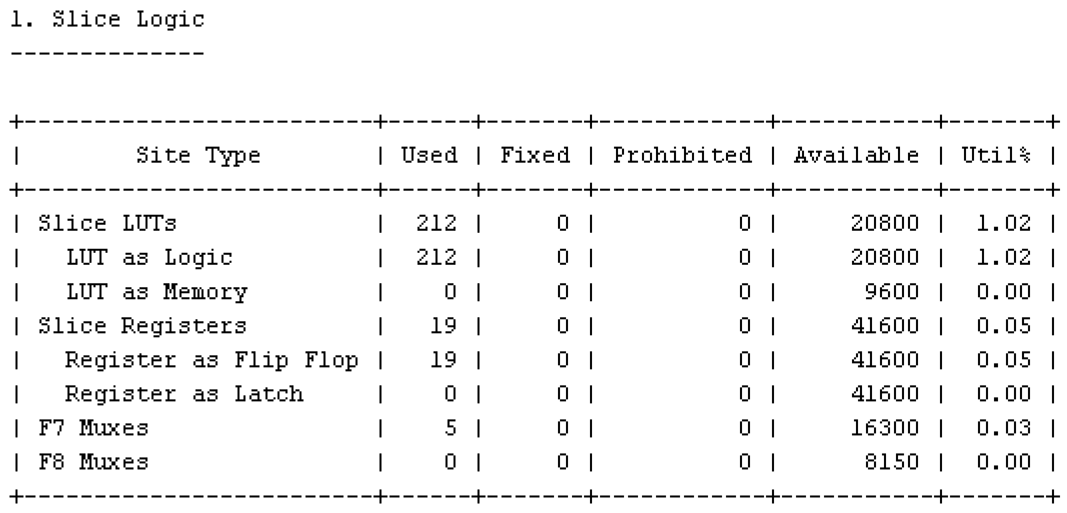


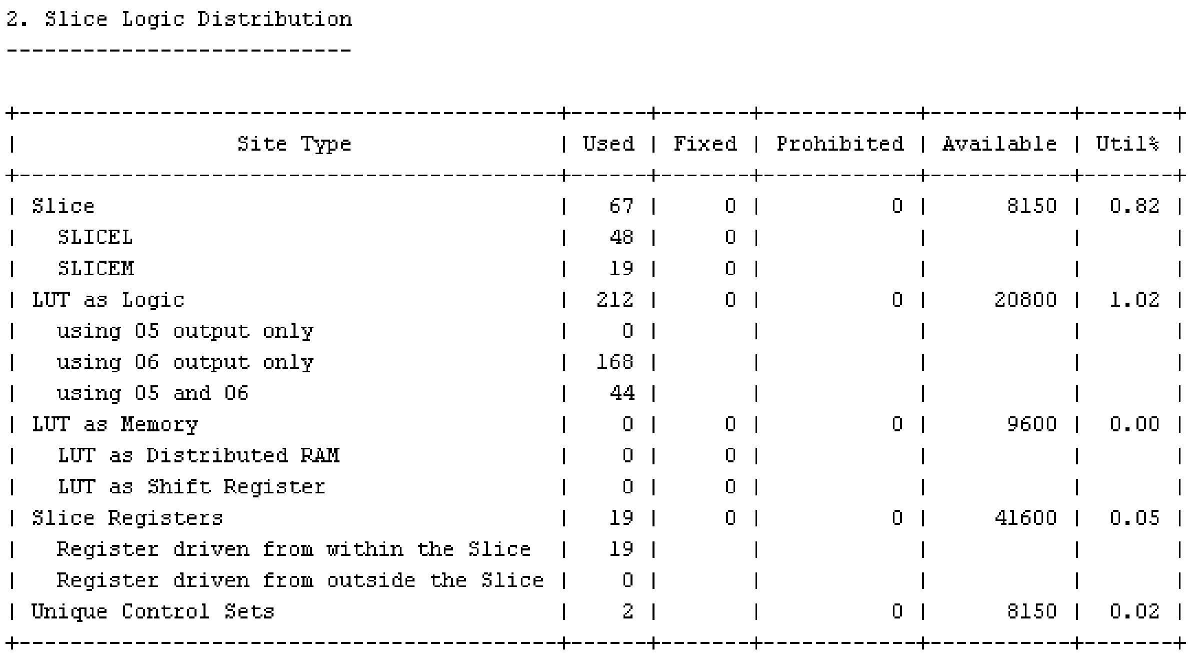
FIG 35 Synthesized schematic diagram

c)Area Utilization Report



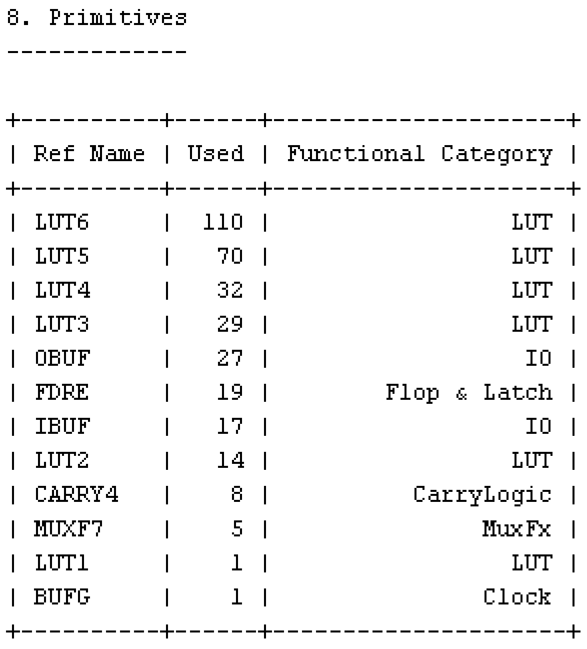
```
1. Slice Logic
--------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs              |  212 |     0 |          0 |     20800 |  1.02 |
|   LUT as Logic          |  212 |     0 |          0 |     20800 |  1.02 |
|   LUT as Memory         |    0 |     0 |          0 |      9600 |  0.00 |
| Slice Registers         |   19 |     0 |          0 |     41600 |  0.05 |
|   Register as Flip Flop |   19 |     0 |          0 |     41600 |  0.05 |
|   Register as Latch     |    0 |     0 |          0 |     41600 |  0.00 |
| F7 Muxes                |    5 |     0 |          0 |     16300 |  0.03 |
| F8 Muxes                |    0 |     0 |          0 |      8150 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
```

FIG 36 LUT Table.



```
2. Slice Logic Distribution
--------------------------

+-------------------------------------------+------+-------+------------+-----------+-------+
|                 Site Type                 | Used | Fixed | Prohibited | Available | Util% |
+-------------------------------------------+------+-------+------------+-----------+-------+
| Slice                                     |   67 |     0 |          0 |      8150 |  0.82 |
|   SLICEL                                  |   48 |     0 |            |           |       |
|   SLICEM                                  |   19 |     0 |            |           |       |
| LUT as Logic                              |  212 |     0 |          0 |     20800 |  1.02 |
|   using O5 output only                    |    0 |       |            |           |       |
|   using O6 output only                    |  168 |       |            |           |       |
|   using O5 and O6                         |   44 |       |            |           |       |
| LUT as Memory                             |    0 |     0 |          0 |      9600 |  0.00 |
|   LUT as Distributed RAM                  |    0 |     0 |            |           |       |
|   LUT as Shift Register                   |    0 |     0 |            |           |       |
| Slice Registers                           |   19 |     0 |          0 |     41600 |  0.05 |
|   Register driven from within the Slice   |   19 |       |            |           |       |
|   Register driven from outside the Slice  |    0 |       |            |           |       |
| Unique Control Sets                       |    2 |       |          0 |      8150 |  0.02 |
+-------------------------------------------+------+-------+------------+-----------+-------+
```

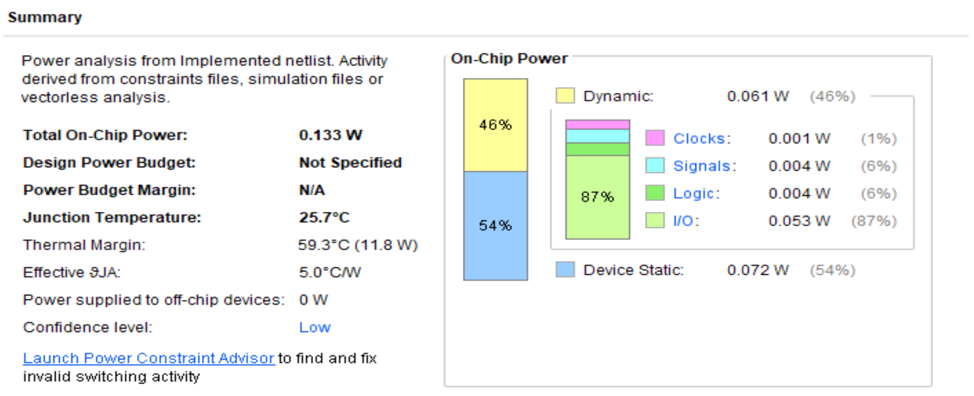
FIG 37 slice logic table



```
8. Primitives
-------------

+----------+------+---------------------+
| Ref Name | Used | Functional Category |
+----------+------+---------------------+
| LUT6     |  110 |                 LUT |
| LUT5     |   70 |                 LUT |
| LUT4     |   32 |                 LUT |
| LUT3     |   29 |                 LUT |
| OBUF     |   27 |                  IO |
| FDRE     |   19 |        Flop & Latch |
| IBUF     |   17 |                  IO |
| LUT2     |   14 |                 LUT |
| CARRY4   |    8 |          CarryLogic |
| MUXF7    |    5 |               MuxFx |
| LUT1     |    1 |                 LUT |
| BUFG     |    1 |               Clock |
+----------+------+---------------------+
```

FIG 38 Logic and memory table

d)Power Report


Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.133 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.7°C**
Thermal Margin:	59.3°C (11.8 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power

Dynamic:	0.061 W	(46%)
Clocks:	0.001 W	(1%)
Signals:	0.004 W	(6%)
Logic:	0.004 W	(6%)
I/O:	0.053 W	(87%)
Device Static:	0.072 W	(54%)

FIG 39 Power Report

5.3 Simulation Output

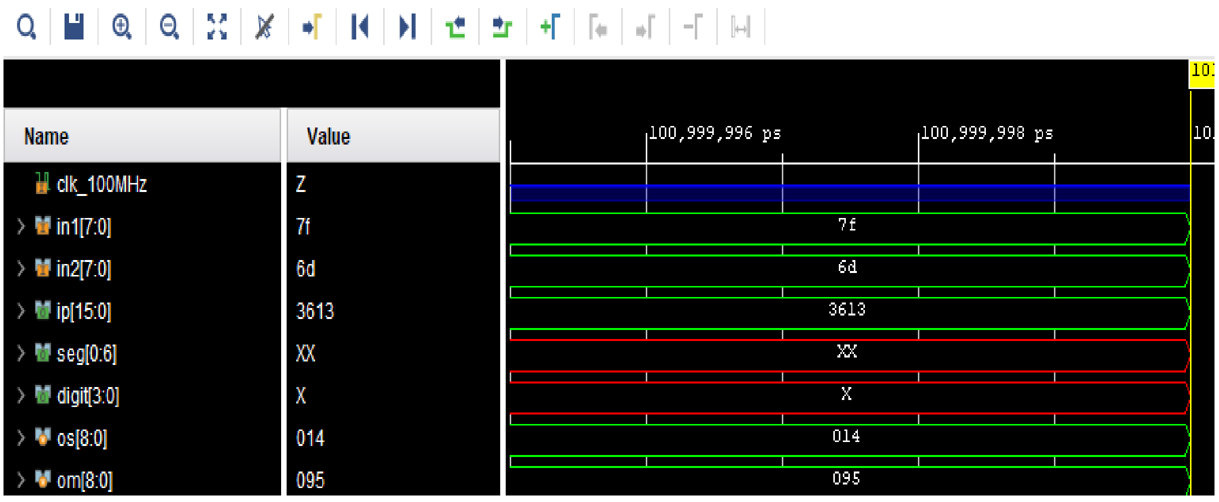
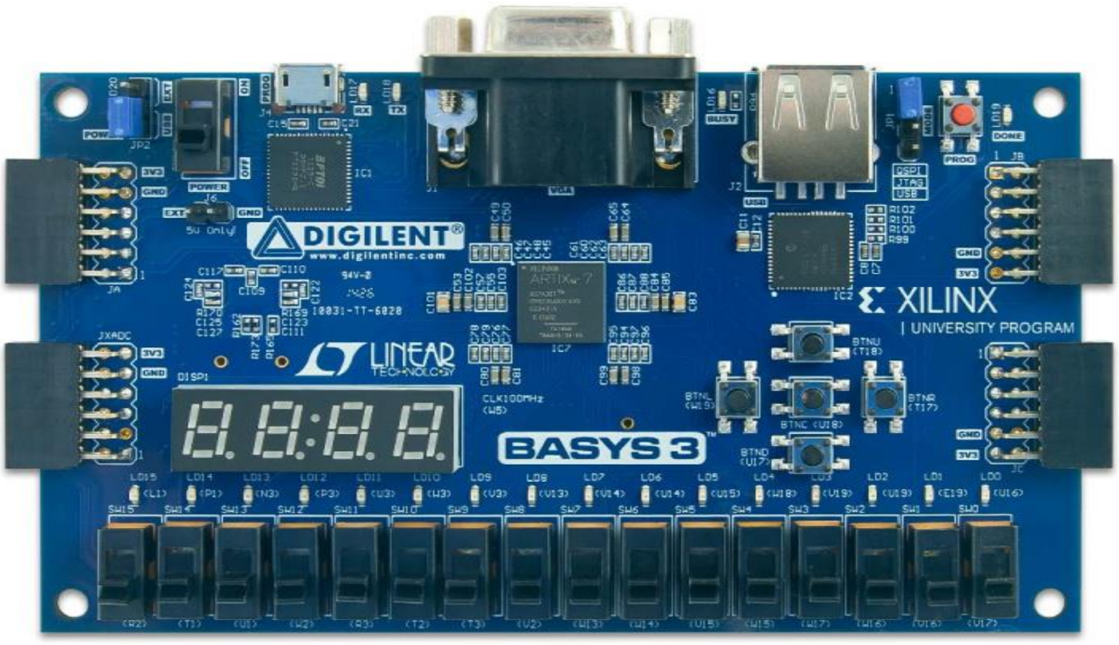
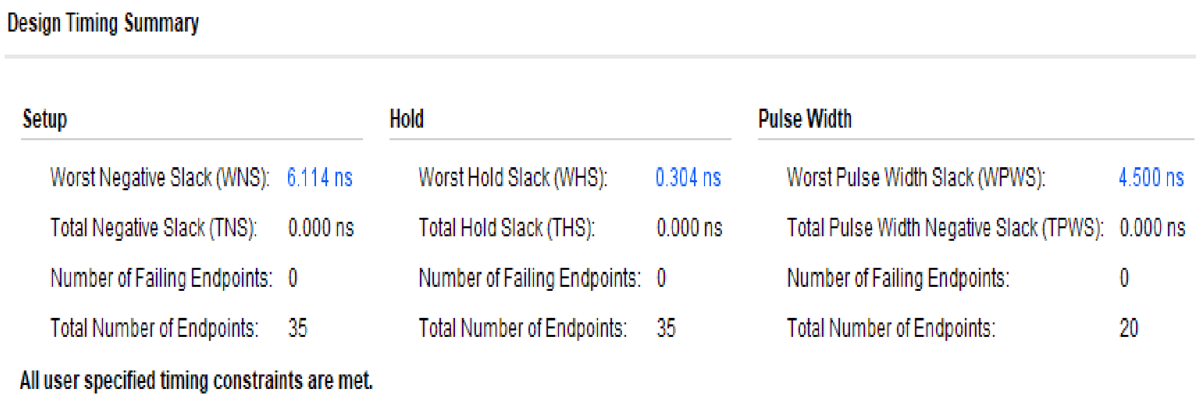

Name	Value
clk_100MHz	Z
in1[7:0]	7f
in2[7:0]	6d
ip[15:0]	3613
seg[0:6]	XX
digit[3:0]	X
os[8:0]	014
om[8:0]	095

FIG 40 Simulation output results

5.4 Hardware Implementation

In this work, all proposed models are implemented on Basys3 Artix7 FPGA with the help of Xilinx Vivado. For implementation first we have to map original input and output ports with board I/Os by generating constraint file. Next, the program can be dumped to FPGA kit to verify the simulation results practically.



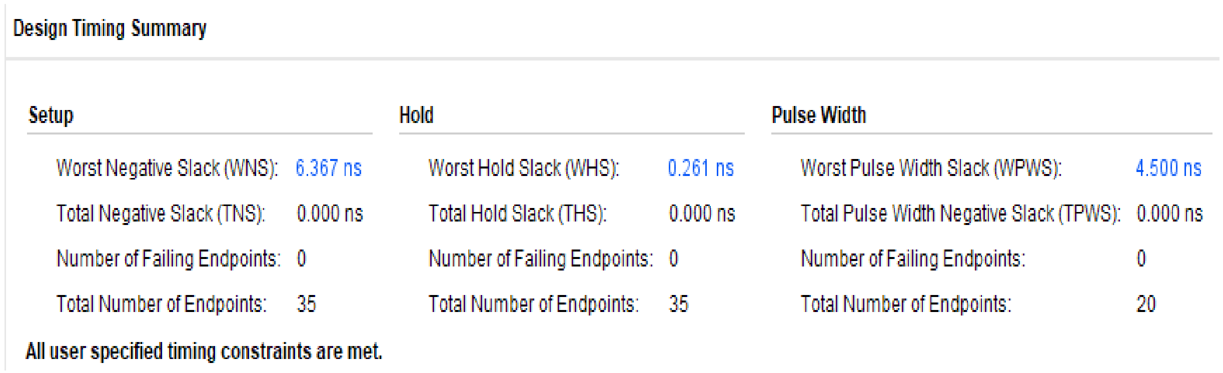


Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.114 ns	Worst Hold Slack (WHS):	0.304 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	35	Total Number of Endpoints:	35	Total Number of Endpoints:	20

All user specified timing constraints are met.

FIG 41 CSD multiplication timing summery.



Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.367 ns	Worst Hold Slack (WHS):	0.261 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	35	Total Number of Endpoints:	35	Total Number of Endpoints:	20

All user specified timing constraints are met.

FIG 42 General multiplication timing summery.

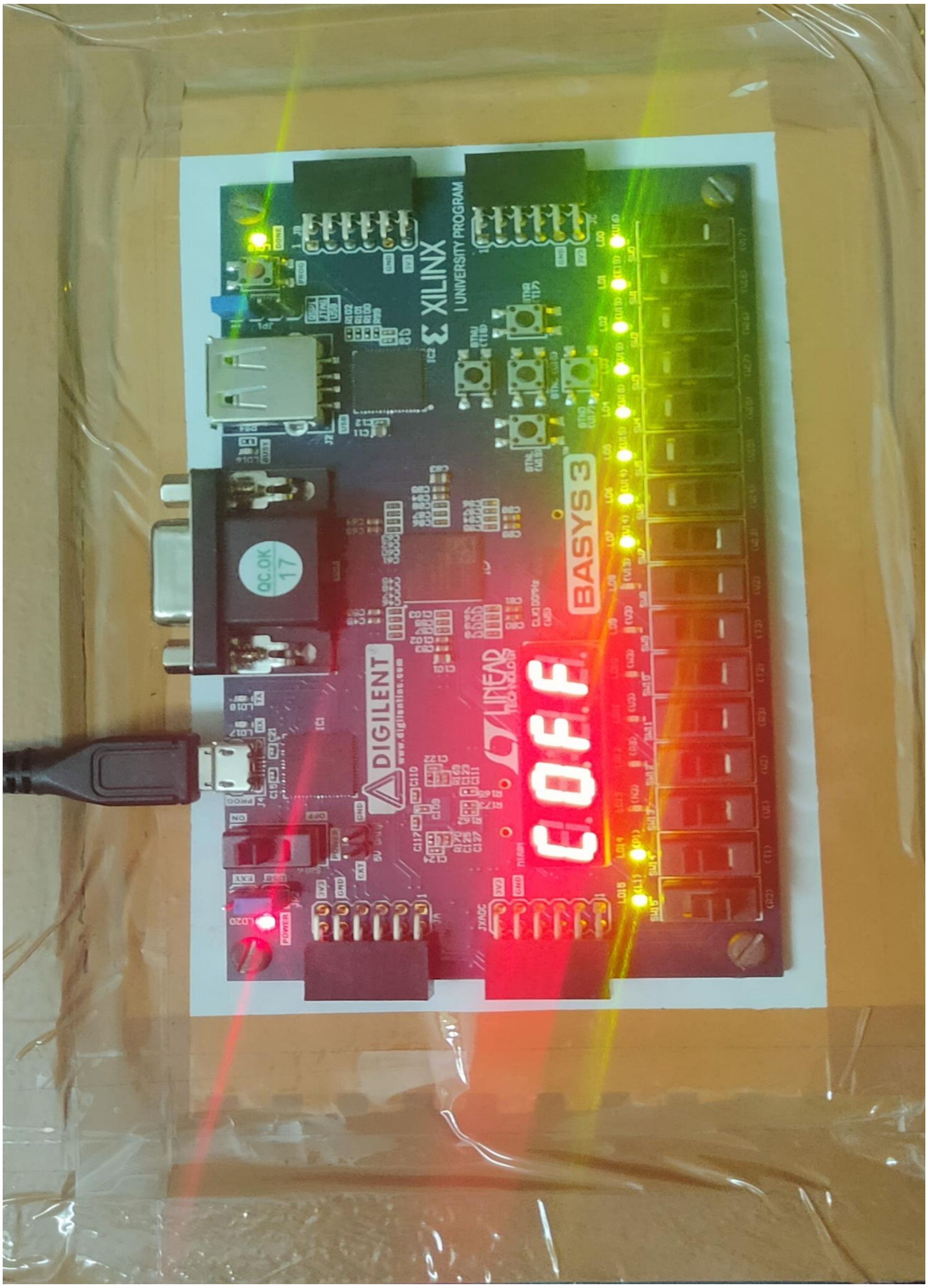


FIG 43 Basys 3 FPGA Kit Output

CONCLUSION

In digital signal processing multiplication is a key operation which determines the overall performance of the multiplier. Using Floating point representation in multiplication makes the operation accurate than using normal multiplication. In this project we have performed floating point multiplication using canonical signed digit algorithm and analysed the power and synthesis results. And we compared the results with normal binary multiplication and we observed that CSD multiplication taking less time compared to General multiplication.

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